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The COTS Technology Authority

VOLUME 2 NUMBER 3
FALL 2006

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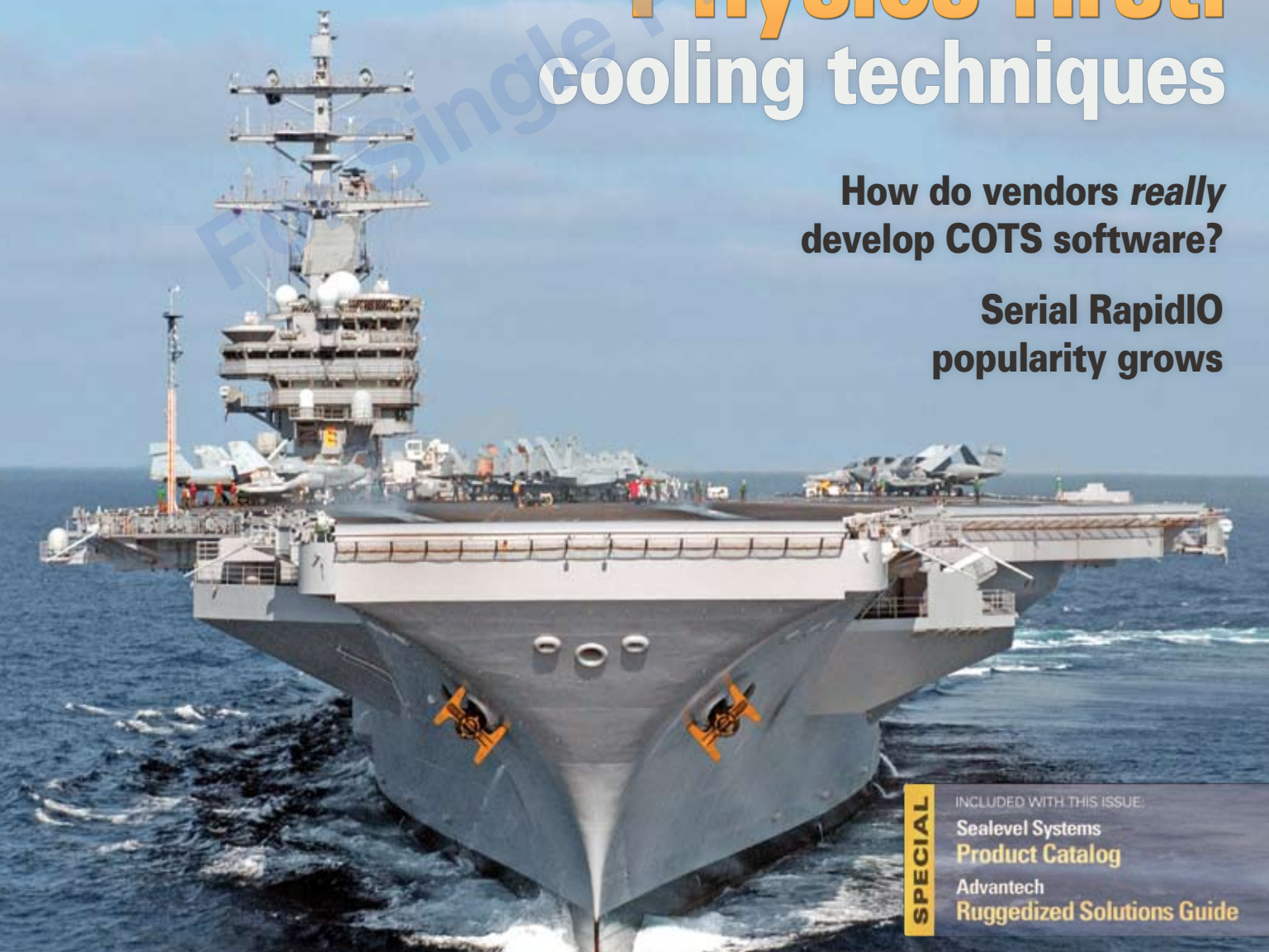

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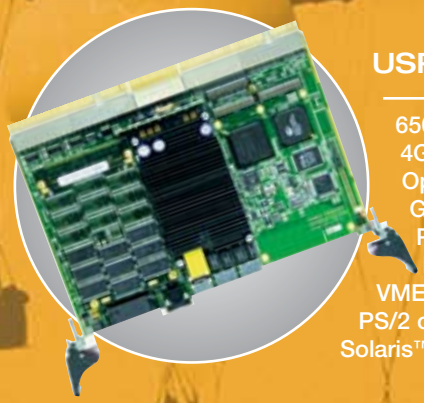

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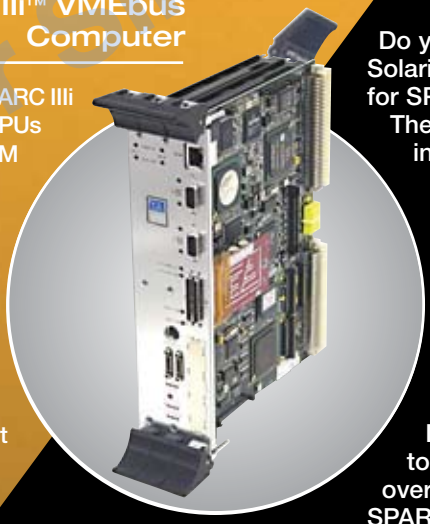

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November 30, 2 p.m. EDT
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"Optimizing DSP algorithims for FPGA implementation," presented by Synplicity
December 6, 2 p.m. EDT
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COVER
The new carrier USS Ronald Reagan (CNV 76) conducts operations off the coast of southern California. You can bet the ship is loaded with COTS hardware and software, from the flight deck bridge to the weapons ops center to the avionics suites controlling her aircraft in flight. But how is COTS software developed? How do designers keep high-performance electronics cool? See articles starting on pages 12 and 38.

(Image courtesy of U.S. Navy, www.news.navy.mil. Photo taken by Mass Communication Specialist 3rd Class Sarah Foster.)

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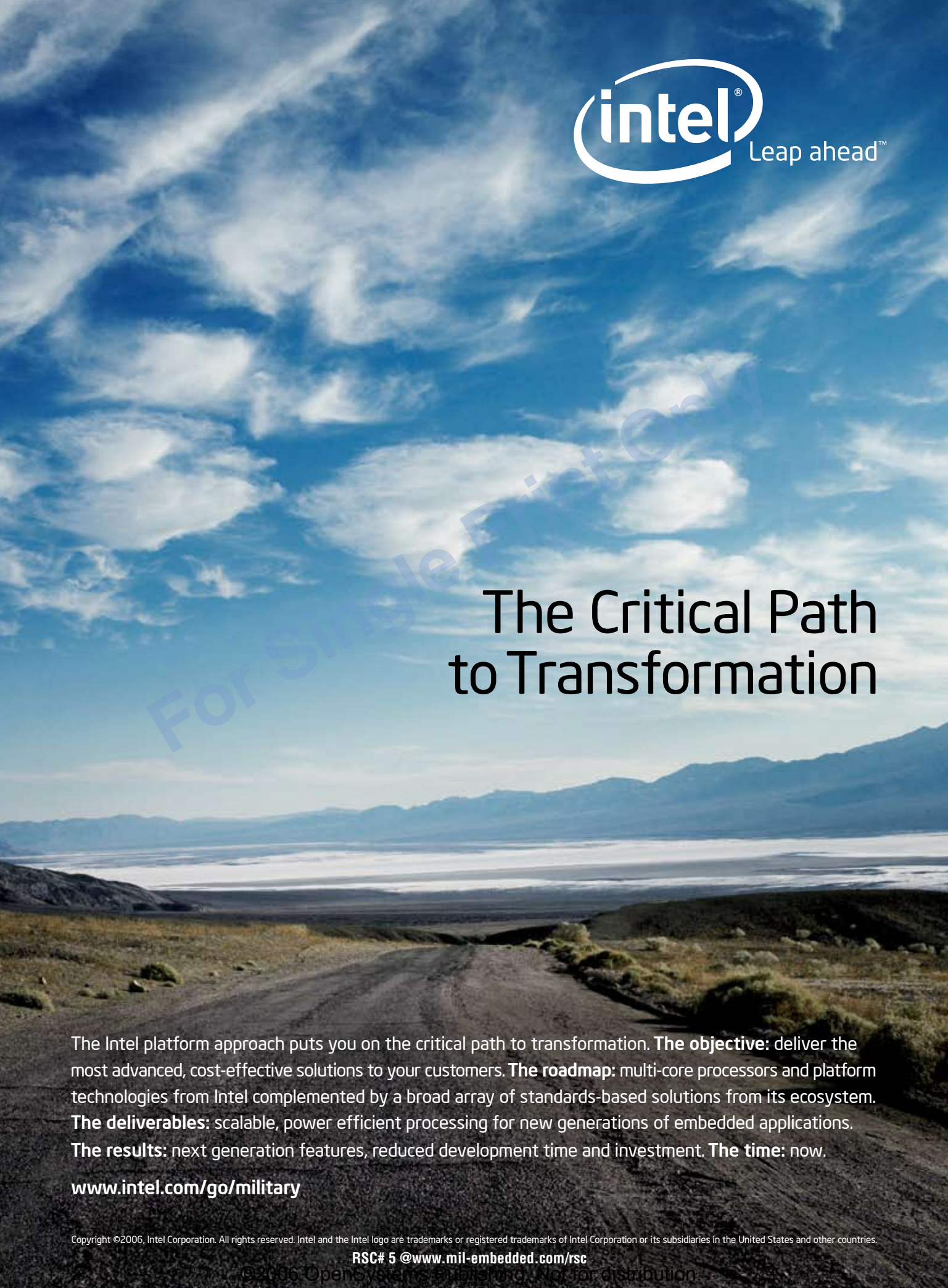

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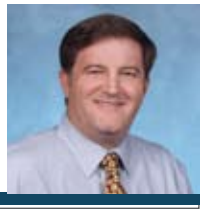

By Jerry Gipper

In the spring of 1981, I was in the final days of my preparation for entry into the real world. The computer labs at Iowa State University were my second home. My first introduction to card buses was the S-100 bus. I was attending demonstrations on emerging PC technology sponsored by Commodore and Radio Shack. I was reading *Byte* magazine when it was still in existence and less than 100 pages!

1981 was a busy year for technology. On April 12, many of us sat on the edge of our seats as we witnessed the launch of Space Shuttle Columbia. After a successful two-day mission, we also watched as it touched down on the long runway at Edwards Air Force Base. (I was in one of those ISU labs.) Since that time, the space shuttle fleet has flown 115 missions.

I also remember using free time to test out those great new video games. Who can forget Frogger, Galaga, and Donkey Kong, all introduced in 1981. I wish I would have used more of that time studying! While we were enjoying these games, we also watched a fledgling cable network – introduced August 1 – that played music on TV: MTV.

On August 12, IBM rolled out the one technology item that has probably had the biggest effect on us techies: the IBM 5150 personal computer. This beige box, with a starting price of $1,565, had a mere 16 kB of memory and used audio cassettes to load and save data. (A floppy disk drive was optional.) IBM's press release trumpeted the screen's "green phosphor characters for reading comfort" and "easily understood operation manuals" that made it "possible to begin using the computer within hours."

IBM's wasn't the first home computer, but Commodore's, Apple's, and Radio Shack's Tandy products were considered "toys." The IBM name added credibility that brought trust to the business environment.

eTForecasts estimates 25-year sales of MS-DOS and Windows PCs based on the original IBM PC architecture:

- ***In the United States:*** Unit shipments have totaled 580 million and represent U.S. $998 billion, August 1981 to August 2006
- ***Worldwide:*** Unit shipments have totaled 1,540 million and represent U.S. $3,100 billion, August 1981 to August 2006

The revenue figures include initial hardware sales only and exclude PC software and services. The software and services sales are probably several times these numbers!

Some of the other computer technology from 1981 that might trigger a memory or two include: the TFC 3450 by Fujitsu, the Commodore VIC-20, the Sinclair ZX81, the Osborne I (who can forget!), the TI-99/4A, the IBM System/23, the Epson HX-20, the Rockwell AIM 65/40 (I cut my teeth on assembly programming on this machine), and the Dynabyte 5100.

In an HP laboratory in Corvallis, Oregon, an Iowa farm-boy-turned-PhD (not me) was about to introduce the HP 12c Financial Calculator. After 25 years, this calculator is still sold under its original name and model.

In late 1981, after several committee meetings and after a number of other companies decided to adopt the combined standard, the NCR BYSE (Byte Serial) and SASI (Shugart Associates System Interface) was introduced under the new name "SCSI."

With all this going on, it's hard to imagine any other great technologies emerging from all the press releases, but it happened! On October 21 (for some reason the numbers 1 and 2 show up in a lot of these introduction dates – maybe this means something to you numerologists out there), there was a small innocuous press release issued from Brussels, Munich, and Hamburg that was to forever change the embedded computing segment of the technology world. The headline declared "Mostek, Motorola, Philips/Signetics, and Thomson CSF announce a common system bus for 16/32-bit computer systems." Of course, they were talking about VMEbus.

The announcing companies were claiming that this technology would be great for process control technology, data technology, intelligent terminals, and digital communication networks.

VMEbus is in some great company. It is a technology that has great staying power, has adapted to the changing needs of its users, and has embraced change as it matures. VMEbus has aged very well. I look forward to the changes that are ahead in the next 25 years.

VMEbus, happy anniversary!

For more information, contact Jerry Gipper at jgipper@opensystems-publishing.com.

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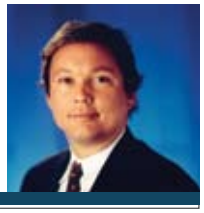
Brilliant inventor or patent troll?



By Jim Turley

Software is a lot like prostitution. You get to sell it, then sell the same thing again to someone else. It's a service industry. There's no inventory, no cost of goods, and no manufacturing problems. It's labor-intensive. There's very little overhead, and the profit margin approaches 100 percent. The *product,* unfortunately, depreciates rapidly with age. And yet, like the world's oldest profession, hardly anyone in the software business – with a few notable exceptions – ever gets rich at it.

Despite all these similarities, most people *like* software companies (again, with one or two exceptions). We look favorably upon the software industry as a beneficial and valuable part of the high-tech community. Nobody seeks to ban software or make it illegal, or to rein in software development or progress. On the contrary, we're training new programmers here and in other countries at a fantastic clip. We want more, please.

Even though there's only a thin line separating these two business models, nobody seems to confuse prostitutes with programmers. We instinctively know the difference between hookers and coders, between women of ill repute and techies of questionable hygiene.

Patents and copyrights are a lot like software, too. There's no tangible product there, but we still know there's real value. We applaud inventors like Thomas Edison for his creative genius and his patented inventions, even though he never actually mass-produced anything. All the light bulbs, phonographs, and what-not were built by other companies under license.

Edison would be less revered if he'd kept all his inventions to himself, hoarding the patents and preventing anyone from making commercial use of them. What good is an invention if no one gets to use it? The whole point of a patent is to promote commercial exploitation; you're *supposed* to share it. Otherwise it's called a trade secret (like the recipe to Diet Coke).

It's good to share, as we learned in grade school. In the high-tech world, it's also profitable. Companies with interesting inventions are encouraged to patent and therefore share them. Companies that can't – or don't wish to – manufacture products can still participate a little in the success of the products they invented.

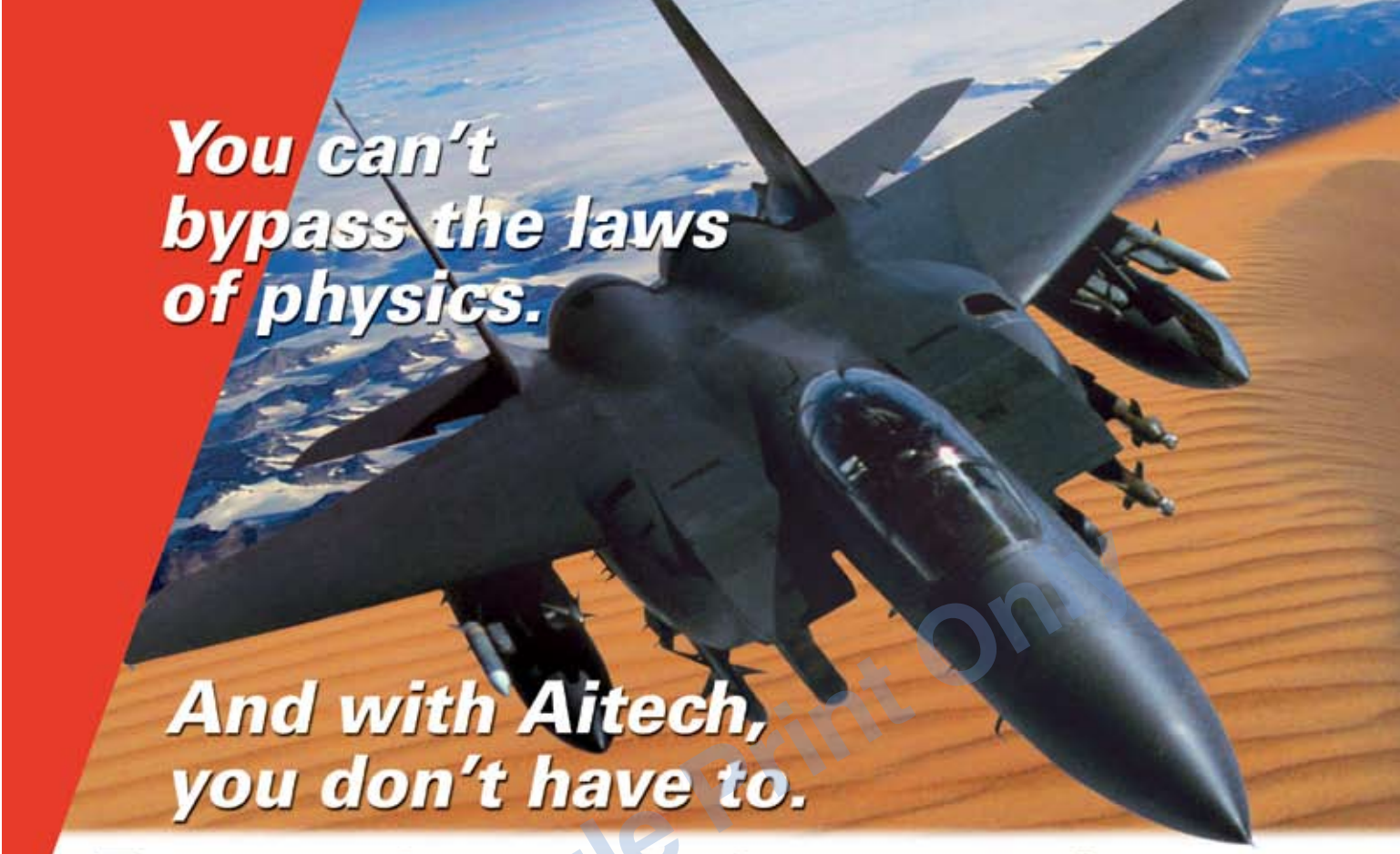
Of course, there's always some risk with sharing. Someone might want to steal your property (intellectual or otherwise) and use it for free. In high-tech patent suits, as in some European soccer games, there's a tendency for one party to fall down and cry "patent troll," shedding alligator tears to gain sympathy and deflect attention away from their illegal behavior.

A real patent troll is a person or company that extorts money for a patent it has no intention of using. An example would be a law firm that buys up patents for no other reason than to milk them for income. That's a lot different from a high-tech company that's been granted its own patents for inventions it developed that were used in its own products and offered for license. Like programmers and prostitutes, there's a big difference between the two, but some observers still tar them both with the same brush.

Yes, Virginia, there really are patent trolls, but they're not lurking under every high-tech bridge throughout the hardware and software landscape. Just because a company enforces its patent rights doesn't make it a patent troll or a bad guy. Jeer at the law firms if you want, but spare a cheer for the high-tech hardware and software companies that have invented things, shared them with the world, and maybe made a living from their inventions.

Jim Turley *is an independent analyst covering microprocessors, embedded systems, intellectual property licensing, and semiconductors. He writes, presents, and consults with high-technology firms throughout the world. He is also a member of the board at Patriot Scientific. Jim is the author of seven books and hundreds of articles. He was previously editor-in-chief of* Embedded Systems Design *magazine and editor of the journal* Microprocessor Report. *He is frequently quoted in* The Wall Street Journal, The New York Times, San Jose Mercury News, *and appears on TV, radio, and Internet broadcasts. He has a stunningly attractive wife, two overachieving children, and an apparently brain-damaged dog.*

For more information, contact Jim at jim@jimturley.com.



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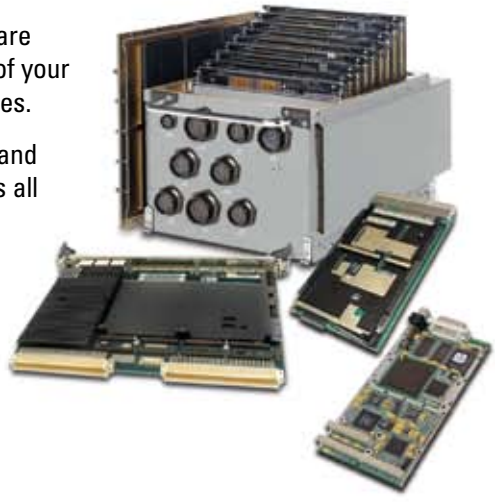

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Improved cooling technologies for both power-supply and motor-drive military applications

By Ralph Remsburg

Power dissipation problems are requiring increasingly complex design solutions. While designs that are more efficient make thermal management possible, current chips and systems still require sophisticated methods for dissipating heat. Several different fin geometries might be used to cool a three-chip, 1,080 W Insulated Gate Bipolar Transistor (IGBT) copper cold plate. The geometries are compared using maximum junction temperature and efficiency. One manufacturing method, Metal Injection Molding (MIM), appears to meet the thermal objectives and is examined more closely.

Insulated Gate Bipolar Transistors (IGBTs) generally are used as switching components in inverter circuits in both power-supply and motor-drive military applications. Although very efficient, these modules suffer from conduction and switching-power losses, which generate heat that must be conducted away from the power chips into the environment.

Previously, familiar air-cooled aluminum heat sinks were sufficient for this heat conduction. But as some military converter and inverter circuit applications reached multi-megawatt requirements, the more thermally effective approach of liquid cooling using copper cold plates has become more common. Cold plates have been improved with more capable designs that utilize lanced-offset fins to replace serpentine-tube cold plates. However, the space constraints of shrinking cold plates – and the strict demand to lower cost – have created a need for even more efficient heat-transfer surfaces within the cold plate.

Innovative designs utilizing impingement flow paths and microchannel surfaces are starting to be used. A manufacturing process called *Model Injection Molding* (MIM) makes highly efficient nonlinear fin arrays. A *fin*, technically referred to as an extended surface, is a protrusion from a heated surface that provides more surface area for heat dissipation. A fin array or fin pattern usually takes the form of a repeating series of identical fins with identical spacing between fins. The exact shape and spacing between fins can have a dramatic effect on the amount of heat that can be dissipated from a surface, and hence, the junction temperature of a device mounted to that surface.

Fin comparison

While there have been many studies of single cooling fin geometry parameters, the conclusions often conflict or can be applied only over a narrow range of variables. A review of the literature reveals that most studies of single-fin geometry neglect the importance of pressure drop, which for most real-world liquid-cooling systems is directly related to thermal performance by the pump flow curve. Even when the literature agrees on the relative performance of a single fin, these findings may become distorted when multiple, identical fin flow fields interact within a fin array.

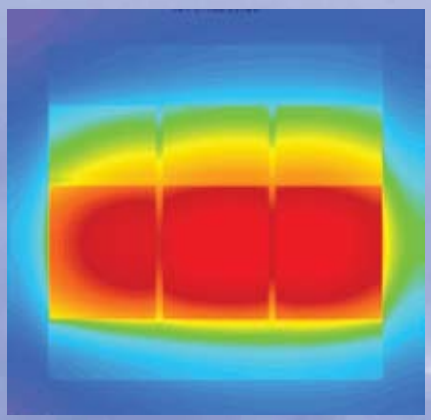

Figure 1

Figure 1 shows a 50 mm x 50 mm IGBT module containing three IGBT chips dissipating 300 W each and three diodes dissipating 60 W each. The total power dissipation is 1,080 W. Simulations were run using seven different extended surfaces to find the best-performing surface in terms of heat transfer coefficient, volumetric efficiency, and use of minimum pumping power.

To simulate the cooling capability of the various fin patterns, Flomerics Inc. Flotherm v6.1 software was used. Flotherm is a Computational Fluid Dynamics (CFD) analysis tool widely used in the electronics-cooling industry. For each simulation, the ambient air temperature is 80 ˚C. Radiation effects are not included in the analysis. The steady-state temperature distribution, fluid velocity, and pressure drop were recorded as the volumetric flow rate was increased from 1 liter/minute to 20 liters/minute. The details of the seven cooling patterns are shown in Table 1. The *x*-axis is parallel to the fluid flow.

Figure 2 shows a thermal comparison of the various fin geometries. The curves represent the maximum semiconductor junction temperature when using a 30 percent EGW mixture having an inlet temperature of 80 ˚C to cool the 1,080 W IGBT module described.

Note that using the double-pass tube has roughly the same temperature result at 20 liters/minute as the staggered square pin pattern has at 1 liter/minute. The nonlinear array shows a lower junction temperature at all simulated flow rates. The single and double pass tubes would probably have unacceptable results in a cooling system unless the system could supply a large volume of coolant at low

Pattern	# Fins in x	# Fins in y	Diameter or thickness (mm)	Fin area (cm^2)
Single tube	-	-	10.0	15.7
Double tube	-	-	10.0	31.4
Stacked fins	49	-	0.20	245
Square in-line	31	31	0.785	151
Square staggered	31	31	0.785	151
Lanced-offset	49	8	0.20 x 3.5	137
Nonlinear	-	-	0.5	135

Table 1

pressure. In this 1,080 W application, the nonlinear array has an 11.2 ˚C lower junction temperature at 1 liter/minute than the next best performing geometry, which is the lanced-offset fin pattern. At 20 liters/minute, the nonlinear array maintains a 2.0 ˚C lower junction temperature.

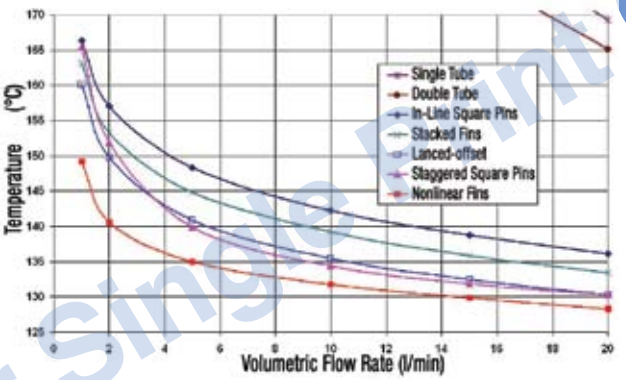

Figure 2

Figure 3 shows a comparison of pressure drop results for the simulation series.

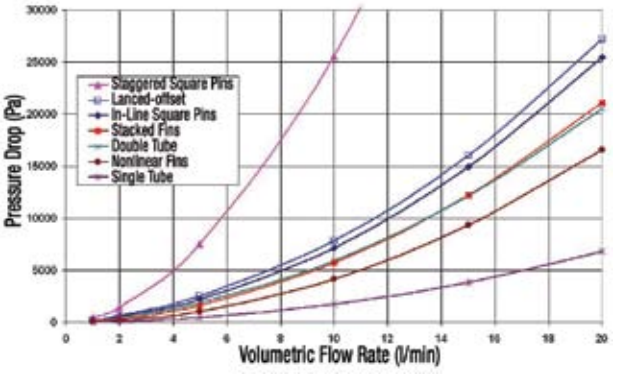

Figure 3

The staggered square pins, although producing a good result in terms of temperature rise (second to the nonlinear array), have a high-pressure requirement. At 20 liters/minute, the staggered square pins have nearly 4.3x the fluid resistance as the nonlinear array.

Figure 4 shows the relative efficiency of the fin patterns when compared using a metric of θP_p which is the product of ˚C/W and watts of pumping power. The lower the value, the more efficient the fin pattern. As noted previously, the staggered pin pattern has

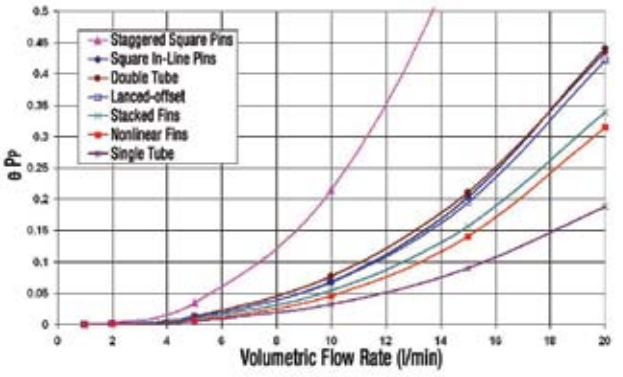

Figure 4

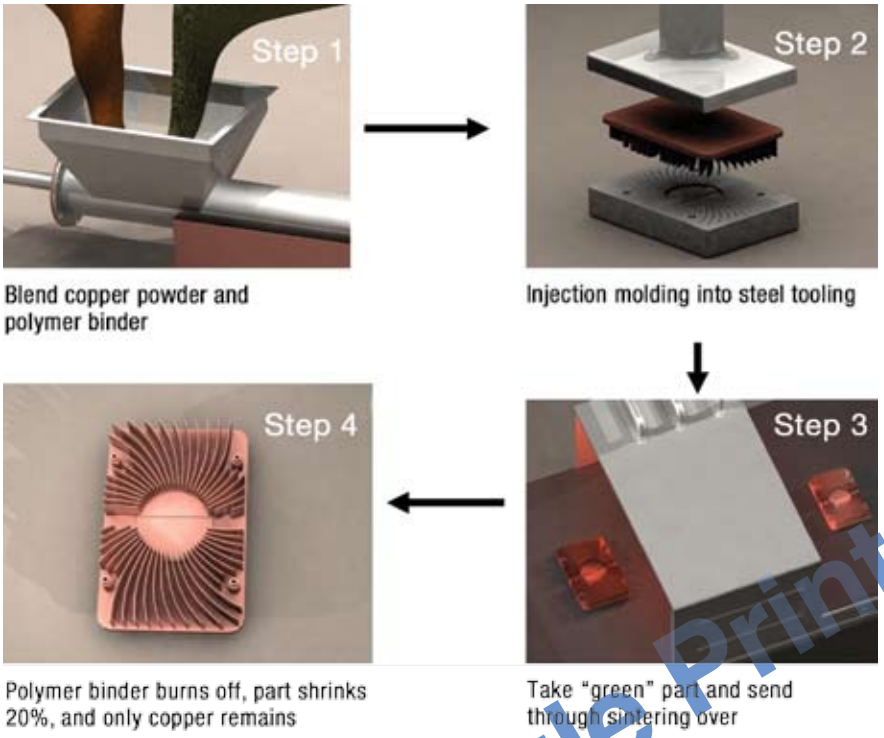

Figure 5

good thermal performance but a very high-pressure drop. Therefore, efficiency is low.

According to data presented in Figure 4, the best surface in terms of efficiency is the single-pass tube. Although the efficiency is high, the lack of surface area and the resulting high junction temperature may preclude the use of this type of cold plate for cooling high-power modules. The nonlinear array performs better than all the other tested configurations in terms of junction temperature and has a relatively low pressure drop and, therefore, high efficiency. Because of the high efficiency, the nonlinear array may have advantages when it's used in low- and high-power applications.

Nonlinear fin arrays

In a nonlinear fin array, extensive CFD analysis ensures that each fin is optimized for maximum performance while simultaneously accounting for the performance flow fields of the fins adjacent to it in the array.

There are only a few processes that can economically produce a nonlinear fin array. MIM is one of the most flexible. Using combined patented and proprietary technology to address thermal management challenges in the computing and other industries, MIM injection-molding technology was developed by Amulaire Thermal Technology.

Figure 5 shows the sequence used to make a MIM part. First, a mixture of powdered metal and polymer binders is molded into the desired shape. The part is removed from the mold and sintered at high temperatures to remove the polymer binders so that no extraneous material remains in the final product. Sintering also bonds the metal particles. During sintering, while the polymer binder debinds and vaporizes, the parts shrink in a uniform and controlled manner. Usually a net shape is achieved with no need of further processing.

Cold plates made using this MIM process can have more pin fins to increase the surface area of the cold plate, and they can have highly complex nonlinear fin patterns. One recently developed cold plate, for example, contained 5,000 pin fins in a 5 x 5 inch area. Amulaire has also designed compact and unique fin pattern solutions for dissipating nearly 6,000 W, utilizing the MIM process, as shown in Figure 6.

Figure 7 shows a top view of the flow field of the optimized nonlinear fin array utilizing an impingement flow pattern used in this simulation. Each fin is individually designed to take advantage of the existing direction of fluid flow,

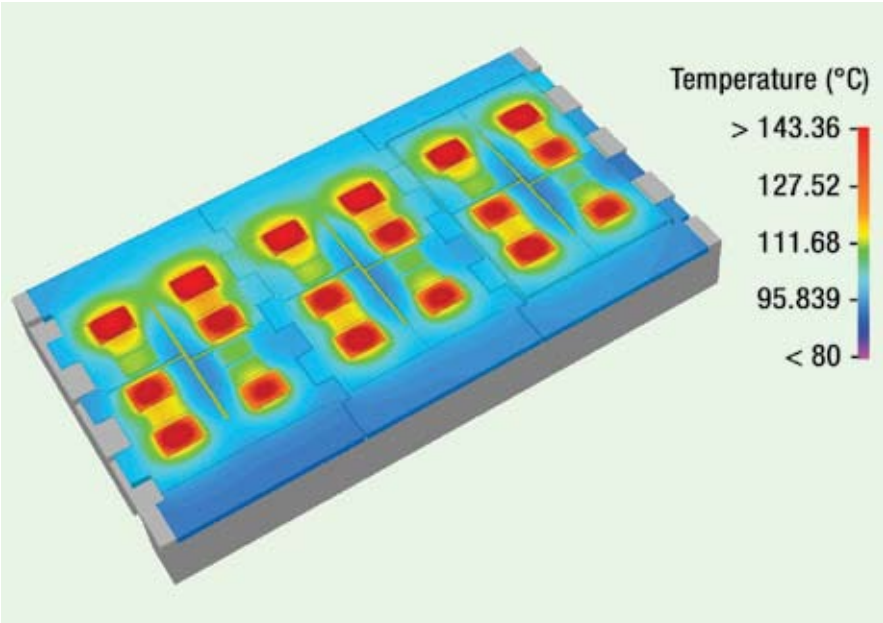

Figure 6

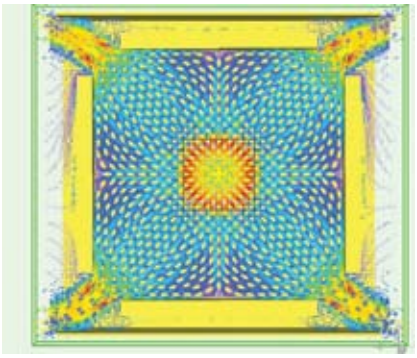

Figure 7

minimizing pressure drop while offering an optimized heat transfer surface area. The inlet coolant flow impinges at the center of the fin pattern. Round pins at the center transfer heat directly from the hottest part of the IGBT module into the fluid area of the cold plate having the highest fluid velocity and highest heat-transfer coefficient.

As the fluid moves outward from the point of impingement and the velocity decreases, the round fins change shape to ellipses to take advantage of the direction of fluid flow and offer more surface area. Although the surface area of each fin is greater in this area, the pressure drop does not increase greatly because the fluid is moving slower.

As the fluid approaches the exit ports, velocity starts to increase. Again the fins change shape, but from elliptical to round. At the same flow rate, this nonlinear design results in a significant reduction in maximum temperature from the lanced offset fin pattern of Table 1, which would be the typical choice used to cool the module. Because the objective of thermal management specialists is to eliminate problems in heat transfer at the component and system levels, these results show that a properly designed heat sink using a nonlinear fin array can make an important contribution to that goal.

Increased reliability and performance

A recently developed MIM technology enables the development of cold plates for IGBTs with superior heat-dissipation capabilities. This new approach to IGBT cold plates has implications for both power-supply and motor-drive military applications.

As component designers work to increase the power capabilities of IGBT modules, it becomes more difficult for system designers to stay below the maximum temperatures specified in the manufacturer's data sheets. As temperatures are reduced, reliability and available performance increase. For example, some data shows that reducing the junction temperature 50 ˚C can lead to a 33x life extension (6,000 cycles at 100 ˚C, 200,000 cycles at 50 ˚C). Increasing the level of fin sophistication from standard machined fins to nonlinear fins can put these levels of performance and reliability within the reach of system designers at a competitive price point.

Ralph Remsburg *is chief engineer at Amulaire Thermal Technology. In addition to having acquired more than 20 years of experience as a thermal specialist, he has written two books on the thermal design of electronic equipment and holds 15 patents.*

To learn more, contact Ralph at:

Amulaire Thermal Technology
11555 Sorrento Valley Road
San Diego, CA 92121
Tel: 858-309-4718
Fax: 858-481-6817
E-mail: ralphr@amulaire.com
Website: www.amulaire.com

Adaptive meshing helps Army develop Future Combat Systems

CFD software models muzzle recoil

By Jerry Fireman

Muzzle brakes are needed to shield the Army's new generation of much lighter combat vehicles from the recoil of guns that are just as powerful as those used on previous generation vehicles. Computer simulation is being used to ensure that the gun's propellant flow does not injure soldiers or damage the vehicle. The key to successfully simulating blast overpressure is Computational Fluid Dynamics (CFD) software that automatically increases mesh density in the area of the blast wave.

Image courtesy of U.S. Army

One of the centerpieces of the Army's Future Combat Systems (FCS) program is the development of new combat vehicles that are only about one-fourth to one-half the weight of the Army's current vehicles, yet capable of mounting guns that are as powerful as the older vehicles' guns. To meet this goal, the new lighter vehicles require muzzle brakes that redirect part of the gun's propellant flow backwards to reduce the gun's recoil. But this redirection must be accomplished while keeping the blast overpressure on the vehicle itself low enough to prevent vehicle damage and injury to nearby soldiers.

> **"The conventional approach to mesh adaption … is not ideal for this problem because it puts more elements on the stronger waves …"**

Testing proposed muzzle brake designs is very expensive and time consuming. The engineers at the Army's Benét Laboratories in Watervliet, New York are therefore using a new generation of CFD software to model the gun's recoil forces and blast pressures for different muzzle brake designs to provide optimized solutions of low recoil force with acceptable blast overpressure. The key to their success in modeling blast overpressure has been the development and use of CFD software that automatically increases the density of the computational mesh in the area of the blast wave to provide the required accuracy while keeping the mesh unchanged in other areas where the increased detail is not needed. With future code improvements, this will help them get the accuracy they need, where they need it, without the expense of excessive computation times.

Replacing the current fleet of combat vehicles

The FCS, the Army's flagship transformation program, is a networked array of systems that uses advanced communications and technologies to integrate the soldier with manned and unmanned platforms and sensors. The Army transformation requirements include the ability to put a combat-capable brigade anywhere in the world within 96 hours, a full division in 120 hours, and five divisions on the ground within 30 days. To meet this goal, FCS will, over time, replace the current fleet of heavy vehicles – the M1 Abrams tanks and M2/M3 Bradley Fighting Vehicles – with a new family of lighter and smaller manned and unmanned ground vehicles and aerial vehicles.

The maximum essential combat configuration weight for the FCS family of systems will be 19 tons. These lighter, smaller vehicles are designed to fit into a C-130-like plane. The C-130 is capable of landing on smaller and less developed landing strips, making

it possible to deliver more vehicles closer to where they are needed. The first FCS unit will be fielded in 2008, with 32 brigades equipped by 2014.

Designing a muzzle brake

The U.S. Army Armament Research, Development and Engineering Center's (ARDEC's) Weapon Systems & Technology (WST)/Benét Laboratories are colocated at the Watervliet Arsenal in upstate New York. Benét has been assigned the responsibility for designing the muzzle brake of the Mounted Combat System (MCS) tank cannon and the Non-Line of Sight Cannon (NLOS-C) artillery cannon, which are designed to replace the Abrams tanks and Paladin artillery vehicles as the Army's primary fighting and artillery vehicles.

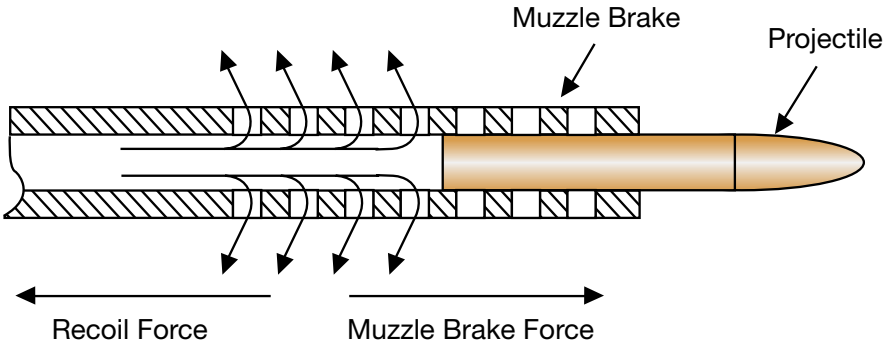

Figure 1

The 19-ton MCS isn't heavy enough to absorb the full recoil force of its 120 mm gun, which fires as powerful ammunition as the 70- to 80-ton Abrams tank. So the MCS will use a muzzle brake to reduce the recoil, a device that is analogous to the thrust reversers that are used to slow down jet airliners after landing. The muzzle brake is a series of holes in the gun tube near the muzzle, through which the gas vents.

Figure 1 depicts a typical perforated muzzle brake operation. As a projectile passes the muzzle brake holes and flow begins to act on the gun tube, a force is generated opposing the recoil force. The venting process pulls the tube forward to counteract the recoil.

The design challenge is to reduce the recoil without putting excessive blast pressure on the vehicle. The challenge is complicated by the fact that a portion of the blast that hits the ground may be redirected back to the vehicle. A blast deflector may be used in an effort to funnel the blast waves coming out of the muzzle brake to the side rather than back towards the vehicle. It is important to be able to evaluate the performance of proposed muzzle brake and blast deflector designs with CFD, because it is expensive to build and test prototypes. Simulation also has the advantage of being able to determine peak pressures generated by exhaust gases at all points on the vehicle so that the vehicle can be designed to withstand them.

Challenges of simulating a blast wave

Despite the advantages that it offers, simulation presents its own special challenges. The motion of the blast wave must be modeled through a large volume of space. Mesh sizes of 0.5 mm or smaller are required at the edge of the blast wave in order to accurately capture the short-lived transients. When the mesh is coarser than this value, it artificially spreads out the blast wave and reduces the accuracy of peak pressure predictions. Having the mesh this fine throughout the entire solution domain, however, would increase the model size to the point where it would have theoretically taken centuries to solve, even on the fastest available computing hardware. Steady-state problems involving steep gradients, such as those occurring at shock fronts, are addressed by using a fine grid in one small region of the computational domain (that containing the most prominent gradients). In this case, however, the steep gradients associated with the blast wave rapidly sweep through the entire domain, so a novel approach is required to simulate the moving blast wave properly.

To overcome this problem, Benét Laboratories is taking advantage of the easy-to-use dynamic adaption capabilities of FLUENT CFD software from Fluent Incorporated, Lebanon, New Hampshire. CFD works by discretizing the flow domain into small cells, the sum of which is called a mesh, so that an algorithm can be applied to simultaneously solve the equations of motion for each cell. Dynamic adaption continually changes the density of the mesh throughout the domain so that as the

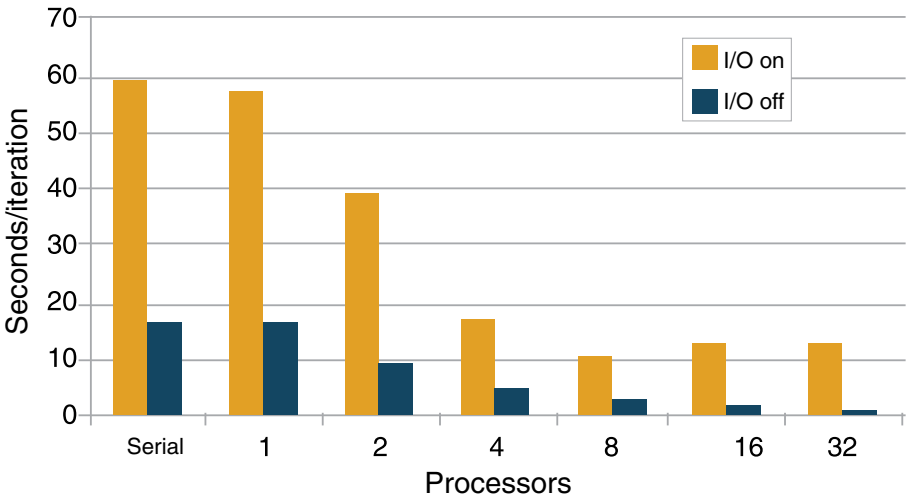

Figure 2

Figure 3

blast wave propagates, the mesh in the area surrounding it is made finer. Regions that were refined earlier in the calculation are coarsened to a reduced mesh density, if the conditions there no longer require the increased detail. FLUENT allows the user to select the criteria upon which the mesh is refined or coarsened. Adaption based on the absolute pressure level has proven most effective for Benét to date, providing sufficient accuracy throughout the model without excessive computation time.

Validation case

In order to validate the accuracy of the simulation, Benét engineers modeled a test rig at the Aberdeen Proving Ground consisting of the gun, mounted on a stand, that will go into the MCS. The simulation was performed on a Linux Networx 32-processor cluster with a Myrinet backbone and METIS load balancing. Engineers configured the zonal adaption capabilities of FLUENT to adapt the mesh every 15 time steps and to increase the number of elements in areas of high pressure by a maximum factor of 32. This simulation began at 1.7 million cells and increased to a peak of 34 million cells through adaption. Figure 2 shows how Linux Networx 32-processor cluster performance increases as more processors are utilized.

The test rig used to validate the simulation is shown in Figure 3. The validation case comparing FLUENT 6.1 results to experimental gun firing for the test is shown in Figure 4. Comparing the simulation predictions to physical testing has shown that CFD accurately predicts the primary or first blast wave peak pressures, but the pressure history below indicates that the CFD results for the peak pressures associated with the waves that are reflected from the ground are lower than the measured values. Furthermore, the

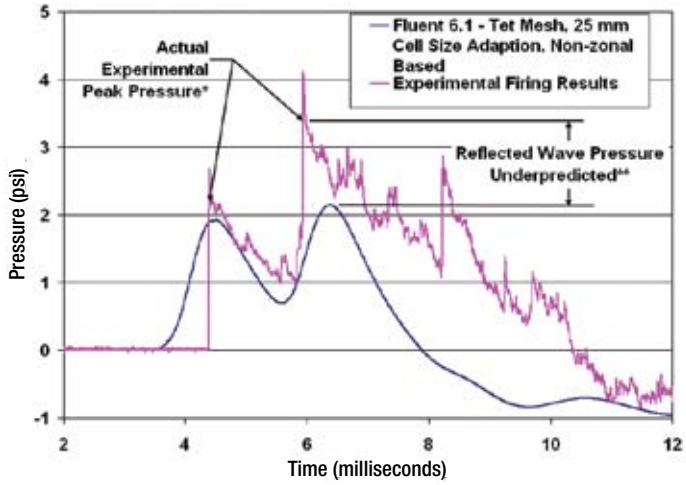

Figure 4

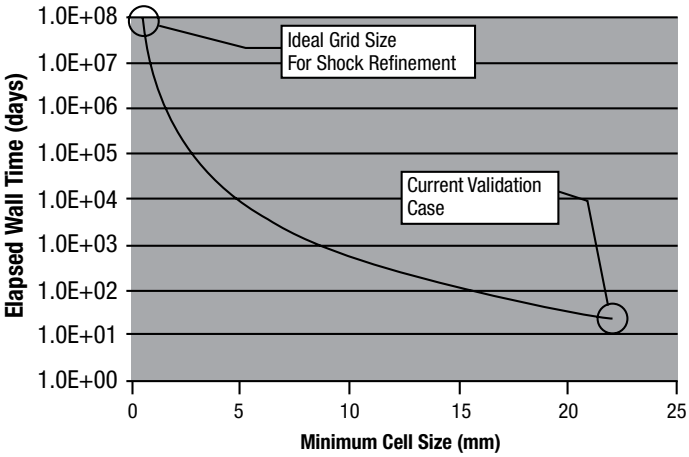

Figure 5

shape of the pressure waves predicted by CFD are much gentler than their measured counterparts. Note the type of pressure transducer used to acquire experimental data overshoots. It is known that the actual pressure is closer to what was predicted in the simulation.

In addition, reflected wave pressures are underpredicted by FLUENT due to lack of mesh resolution. A more finely resolved mesh would yield higher peak pressures and steeper waves, but there is always a trade-off between accuracy and computational expense. For example, had this validation been performed with a significantly finer adapted mesh resolution, such as with a minimum cell dimension of 0.5 mm instead of 25 mm, the calculation would have taken many years.

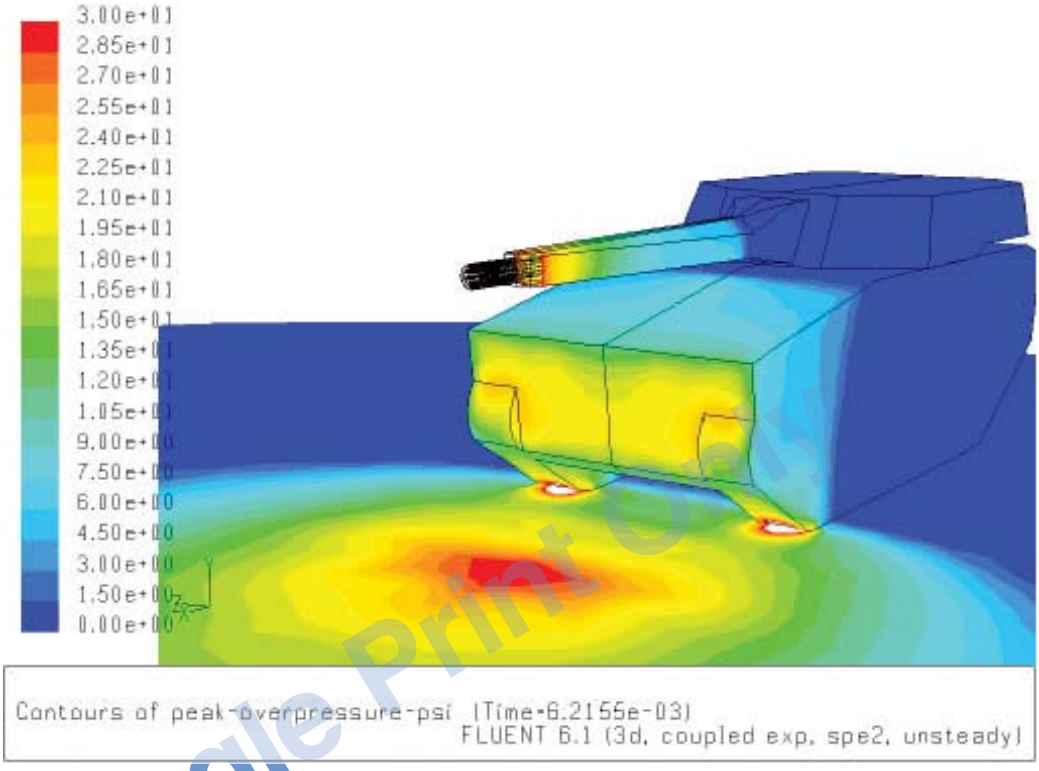

Figure 6

The chart in Figure 5 shows how an increase in mesh resolution to the ideal size would increase solution time to centuries. This problem is addressed with mesh adaption. The conventional approach to mesh adaption, which adapts the mesh based on a fixed criterion throughout the entire flow domain, is not ideal for this problem because it puts more elements on the stronger waves that move forward out of the muzzle and fewer elements on the weaker but more important waves coming out of the muzzle brake and moving back toward the vehicle. Most recently, Benét has been using a new version of FLUENT that allows users to set different criteria for adaption in different areas of the computational domain. This so-called *zonal-based adaption* has demonstrated advantages by making it possible to focus computing resources on the most important sections of the blast wave – those moving toward the vehicle.

But even without zone-based criteria, the CFD analysis via dynamic adaption was found to yield reliable results. With the model having been validated, Benét engineers are using it to evaluate alternative design configurations. For example, Figure 6 shows CFD results with the muzzle brake installed. The results of each simulation show peak pressure levels on the vehicle and can easily be animated to show the movement of the blast wave over time. This capability, which makes proposed changes easier to evaluate, will dramatically reduce the amount of time required to design the next-generation gun for the Army's number one fighting vehicle.

Jerry Fireman *is president and founder of Structured Information, a marketing communications firm representing Fluent Inc. and Benét Laboratories. Jerry can be reached at jerry_fireman@strucinfo.com.*

This article was written with input from Dan Cler, Senior Mechanical Engineer, Benét Laboratories, Watervliet, New York and Christoph Hiemcke, Senior Business Services Engineer, Fluent Inc., Lebanon, New Hampshire.

For more information, contact:

Fluent Inc.
10 Cavendish Court
Centerra Resource Park
Lebanon, NH 03766
Tel: 603-643-2600
Website: www.fluent.com

Benét Laboratories
Technology Transfer Office
10 Buffington Street
Watervliet, NY 12189
Tel: 518-266-4325
Website: www.benet.wva.army.mil

Using resource partitioning to build secure, survivable military systems

By Paul N. Leroux and Kerry Johnson

Network-centric warfare relies heavily on interconnected platforms, weapons, communications, and sensor systems. Of course, each of these "system of systems" contains its own intelligence, which also makes each vulnerable to software glitches, malicious attacks, or simply buggy code. One way to assure that a problem in one system doesn't affect the entire Global Information Grid (GIG) is to use partitioned operating systems. In addition, partitioned environments also offer protection from priority inversions, resource starvation, and other inadvertent but not uncommon software behavior.

By providing access to accurate, timely information from virtually any location, the GIG promises to help war fighters identify and eliminate enemy threats with unprecedented efficiency. Nonetheless, the GIG mandate of networking all military systems will inevitably introduce its own threats, including viruses, Denial-of-Service (DoS) attacks, and other forms of cyber sabotage. To contain such attacks and ensure constant availability of mission-critical services, partitioning provides every software subsystem with a guaranteed share of computing resources.

Limited resources

Safeguarding the reliability and security of net-centric warfare systems represents a significant challenge – a challenge made all the more difficult by the complexity of modern software. This complexity can undermine reliability for the simple reason that the more code a system contains, the greater the probability that coding errors or unanticipated software interactions will make their way into the field. It can also compromise security because hackers typically exploit such errors when they wish to damage or infiltrate a system. Unfortunately, no amount of testing can fully eliminate these problems, as no test suite could possibly anticipate every scenario that a complex software system may encounter.

The process of developing software for military systems presents a further complication. An integrator building a ground-vehicle system, for example, may need to integrate application programs from one vendor, protocol stacks from another, an RTOS from yet another, and an embedded database from still another. The integrator must then combine those components with multiple software subsystems developed in-house, each written by a separate development group. Figure 1 shows some of the many software components that such a system may comprise.

Given the parallel development paths, performance problems invariably arise at the integration phase, when, for the first time, the various subsystems begin vying with one other for CPU time and other system resources. Subsystems that worked well in isolation now respond slowly, if at all. Unfortunately, many of these issues emerge only during integration and verification testing, when the cost of software redesign and recoding is at its highest.

To maintain secure operation and integrate multiple software subsystems successfully, the integrator must implement an architecture that prevents any component or subsystem from corrupting or monopolizing the computing resources (for example, memory and CPU time) that other subsystems require. Integrators could, in theory, achieve this goal by using hardware partitioning, an approach that uses a separate board or node to run each software subsystem or group of subsystems. Such an approach can both contain faults and reduce competition for shared resources. In military systems, however, the trend is toward integrating more

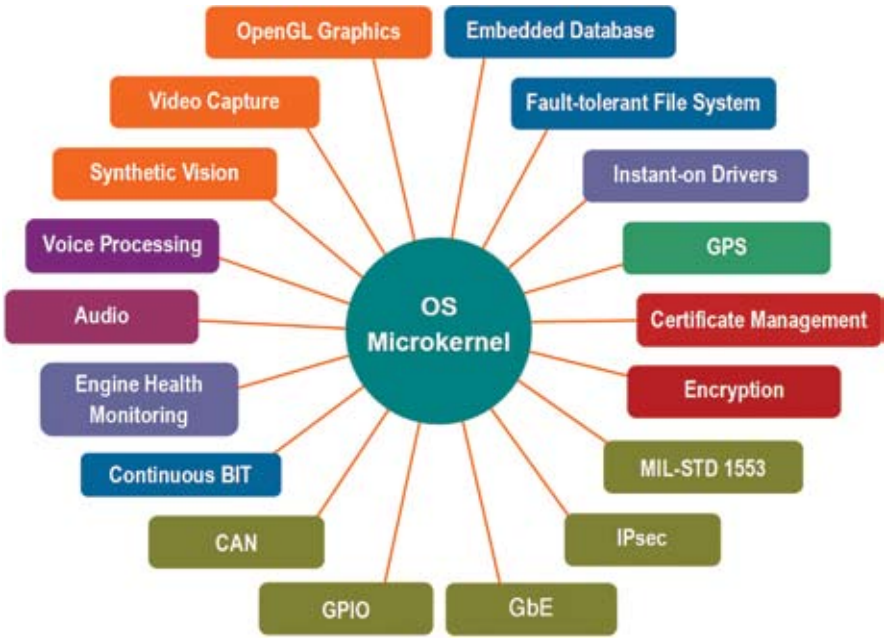

Figure 1

functionality into a single slot. Such an approach not only cuts costs ("saving slots saves money"), but also minimizes weight and power consumption.

Secure compartments

To address these security and integration issues, some designs place virtual compartments, or *partitions*, around groups of software processes and allocate a predetermined set of resources, including CPU time, to each partition (Figure 2). The system can thus prevent processes in any partition from inadvertently or maliciously monopolizing resources needed by processes in other partitions. In the Defense and Aerospace (D&A) industry, many partitioned systems comply with the ARINC 653 specification, which provides a well-known though somewhat rigid and inefficient approach to resource partitioning.

Among other things, partitions can provide memory protection where the OS uses the Memory Management Unit (MMU) to control all memory access. A microkernel operating system, for instance, can partition applications, device drivers, protocol stacks, and file systems into separate, memory-protected processes. If any process, such as a device driver, attempts to access memory outside of its process container, the MMU will notify the OS, which can then terminate and restart the process.

This approach offers an immediate and measurable improvement to system reliability:

- Prevents coding errors in any process from corrupting other processes or the OS kernel
- Allows the developer to quickly identify, diagnose, and correct violations that could otherwise take weeks to isolate
- Reduces fault-recovery times dramatically: Rather than having to reboot when a memory violation occurs, the system can simply restart the offending process

Avoiding task starvation

Nonetheless, building a reliable system involves more than partitioning functionality into separate memory domains. For many systems, ensuring resource availability is also critical. If a key subsystem is deprived of CPU cycles, for example, the services provided by that subsystem will become unavailable to users. In a DoS attack, for instance, an external system could bombard a device with requests that need to be handled by a high-priority process. That process will then overload the CPU and starve other processes of CPU cycles, making the system unavailable to users.

Also, in many cases, adding software functionality to a system can push it "over the brink" and starve existing applications of CPU time. Historically, the only solution was to either retrofit hardware or redesign software.

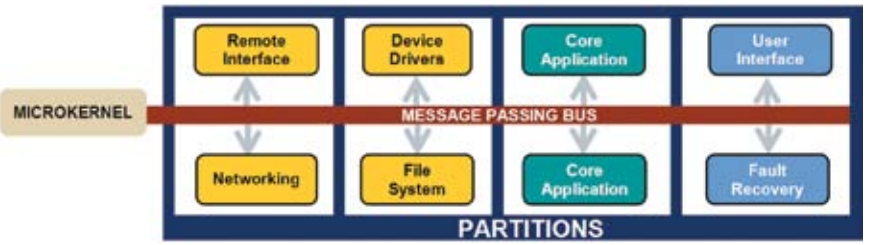

Figure 2

Fixed partition schedulers

To address these problems, some operating systems offer a fixed-cycle partition scheduler, typically based on ARINC 653, that allows the system designer to group processes into partitions and to allocate a percentage of CPU time to each partition. With this approach, no process in any given partition can consume more than the partition's statically defined percentage of CPU time (for instance, 20 percent of the CPU).

Fixed-cycle schedulers have their drawbacks, however. Since the scheduling algorithm is fixed, partitions that aren't busy consume their allocated CPU cycles in an idle state. Meanwhile, other partitions can't access those unused cycles, even when they are busy and could benefit from the extra processing time. This approach squanders valuable (and available) CPU cycles and prevents the system from handling burst demands. Because of this "use it or lose it" approach, fixed partition schedulers can achieve only 70 percent CPU utilization.

Partitioning on multicore processors

Like systems in every other industry, mission computers and subsystems for radar, flight control, and sensor fusion are growing in complexity, with a voracious appetite for computational power. Multicore processors offer the ideal performance upgrade for such systems by delivering significantly greater performance per watt, ounce, and square inch than conventional uniprocessor chips. In fact, system designers will have little choice but to embrace multicore technology, since it forms the basis of most new processor designs.

Thus, an operating system must be able to support resource partitioning on multicore hardware. Unfortunately, most legacy RTOSs, including those with partitioning schedulers, can control only one CPU or processor core at a time. Developers must, as a result, run a separate copy of the RTOS on each core of the multicore chip. Because neither copy owns the entire system, the application designer, not the OS, must handle the complex task of managing the chip's shared hardware resources, including physical memory, peripheral usage, and interrupt handling. To avoid this complexity, systems designers should choose an RTOS that can control multiple cores simultaneously, manage shared resources, and provide dynamic load balancing across cores – while still enforcing resource guarantees.

This cap on CPU utilization presents several undesirable choices to the system designer: Use a faster, hotter, more-expensive processor; limit the amount of software functionality that the system can handle; or simply tolerate slower performance. The cap also presents a "double whammy" to designs that must keep a significant percentage of CPU cycles in reserve for future applications or system enhancements.

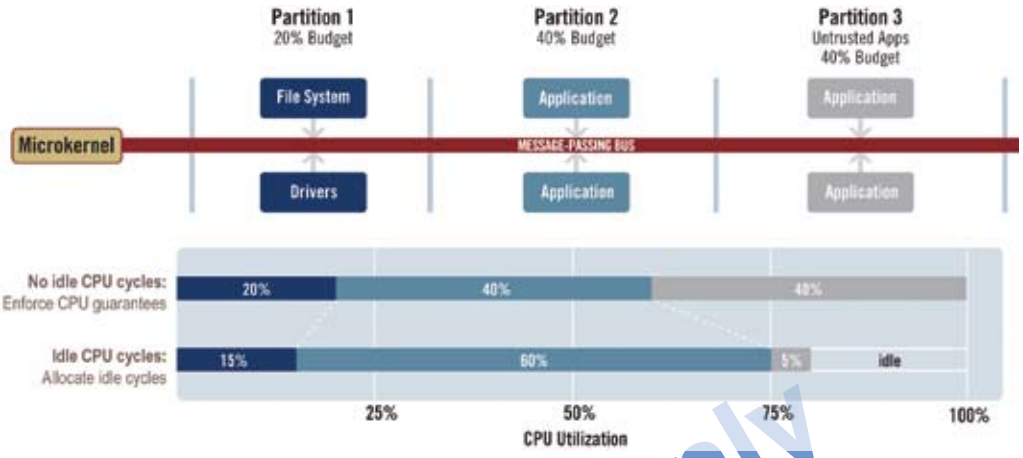

Figure 3

Also, to request OS services or to communicate with other processes, applications must use the APEX interface as defined in the ARINC standard. This restriction prohibits legacy applications from leveraging the benefits of secure partitioning.

Adaptive partitioning schedulers

Another approach, called *adaptive partitioning,* addresses these drawbacks by providing a more dynamic scheduling algorithm. Similar to fixed-cycle partitioning, it allows the system designer to reserve CPU cycles and memory for a process or group of processes. Designers can thus guarantee the load on one software subsystem won't affect the availability of other subsystems.

Unlike fixed approaches, however, adaptive partitioning recognizes that CPU utilization is sporadic and that one or more partitions can often have idle time available. Consequently, an adaptive partitioning scheduler will dynamically reallocate those idle CPU cycles to partitions that can benefit from the extra processing time. This approach, which was pioneered by QNX Software Systems, offers the best of both worlds: It can enforce CPU guarantees when the system runs out of excess cycles (for guaranteed availability of applications and services) and can dispense free CPU cycles when they become available (for maximum CPU utilization and performance). In Figure 3, for example, Partition 2 consumes no more than 40 percent of CPU cycles when the system is running at capacity. But it can consume more than 40 percent whenever other partitions require less than their allocated CPU budget.

Adaptive partitioning offers several other advantages, including the ability to:

- Use real-time, priority-based scheduling when the system is lightly loaded, allowing systems to use the same scheduling behavior that they do today
- Overlay the partitioning scheduler onto existing systems without code changes, enabling users to launch existing POSIX-based applications in a partition
- Achieve 100 percent CPU utilization in a controlled fashion, allowing integrators to realize the benefits of time partitioning without the need for faster, more expensive processors
- Guarantee that fault-detection and recovery operations have the CPU cycles they need to repair software faults, thereby improving Mean Time To Repair (MTTR)
- Allow operators to remotely monitor or troubleshoot the system without interrupting the availability of critical applications
- Stop malware and DoS attacks from stealing all available CPU time

While adaptive partitioning offers greater flexibility, fixed-cycle scheduling may be desirable in some situations. To address this requirement, an implementation of adaptive partitioning should allow the system designer to configure a system with fixed partition budgets and no CPU time "borrowing." This approach frees system designers to choose the most appropriate scheduling behavior for their application requirements.

Conflicting demands

Embedded software is becoming so complex that, without some form of partitioning, system designers and software engineers will be hard-pressed to satisfy the conflicting demands for reliability, performance, security, time to market, and new features.

With resource partitioning, vendors can readily integrate subsystems from multiple software teams, subcontractors, and third party developers; allow new and upgraded components to run without compromising existing system behavior; and contain the effects of DoS attacks and other network-based exploits. If the partitioning solution also provides a flexible, efficient scheduler that allows 100 percent CPU utilization, then vendors can realize these benefits without having to incur the cost of faster, more expensive hardware.

Kerry Johnson *is a senior product manager at QNX Software Systems, where he is responsible for product road maps and introducing new technology to the embedded market. He has 20 years' experience as a software design manager and project manager in companies such as Nortel, CrossKeys, and Research in Motion. He holds a Bachelor's of Applied Science in Electronic Information Systems Engineering from the University of Regina, Saskatchewan.*

Paul Leroux *is a technology analyst at QNX Software Systems whose interests include high availability design, multiprocessing systems, and OS kernel architecture.*

For more information, contact Paul or Kerry at:

QNX Software Systems
175 Terence Matthews Crescent
Ottawa, Ontario Canada, K2M 1W8
Tel: 613-591-0931
E-mail: info@qnx.com
Website: www.qnx.com

Using your existing test and measurement platform to perform Serial RapidIO protocol analysis

By Barbara Aichinger

The Serial RapidIO (SRIO) standard is now meeting the need for increased bandwidth, lower latency, and faster interconnect speeds. But with increased performance comes new challenges in the validation and debug phases of product development. As design engineers migrate their skill sets from standard to standard, they also must migrate their lab debug skills and equipment to accommodate the newer, faster technologies. Do engineers need to go out and invest and learn a new set of tools? The surprising answer is "no."

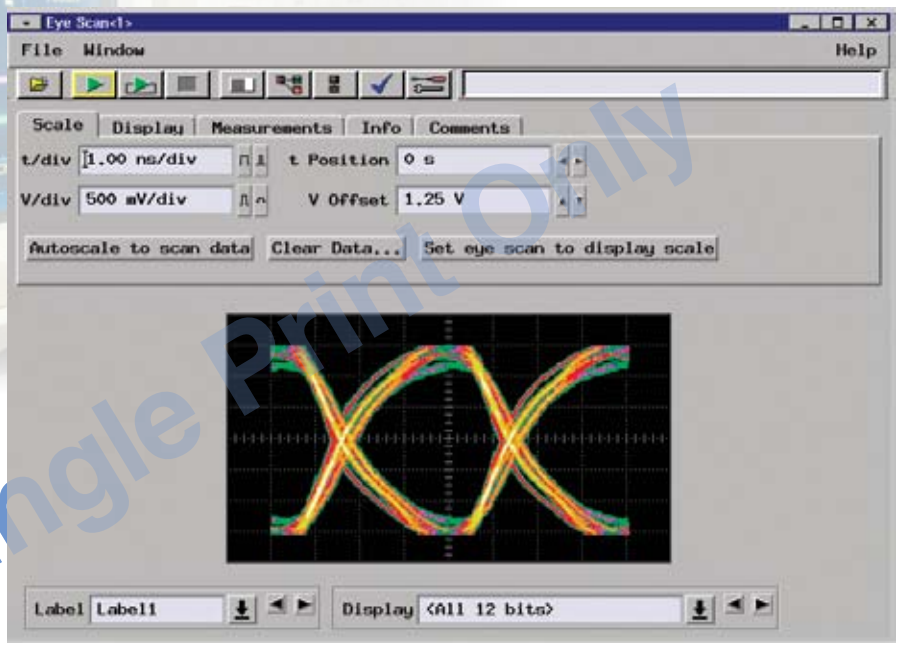

Figure 1

Design validation of parallel buses is challenging but fairly straightforward. Parallel buses by nature are made up of an address bus, a data bus (sometimes multiplexed), control signals, and a clock. More sophisticated high-speed parallel buses may even contain several clocks, thus creating multiple time domains. The tools that engineers use to validate these buses are available and are a fairly close match, architecturally, to the task of attaching and decoding parallel buses. These tools are generally scopes and logic analyzers.

> **"The digital oscilloscope with its low channel count and high-speed sampling can still be used for serial interconnect debug ..."**

In many cases, specialized hardware and software for parallel bus analysis are available that attach to and run on a scope or logic analyzer to help with protocol decode and timing analysis. However, even in the absence of these specialized add-ons, engineers could observe parallel buses with just high-speed sampling. Armed with a timing diagram and the general output of the logic analyzer or scope, engineers could still get a rough idea of what was going on.

But serial interconnects are different. Since the data is encoded and involves clock recovery, simple high-speed data sampling reveals only eye diagrams (see Figure 1).

These serial interconnects such as Serial RapidIO are replacing parallel buses in today's systems; however, the function that these interconnects provides remains largely the same: They move data quickly and efficiently from one functional area to another. For design validation and debug, engineers still have the same issues including:

- Checking for general system integrity
- Looking for protocol errors to ensure specification compliance
- Finding events that lead up to a system hang up or lockup
- Measuring performance through devices

With the advent of serial interconnects changing the overall computer architecture landscape, what will engineers do with their general purpose, parallel-bus-oriented test equipment?

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Photo courtesy of USN

The digital oscilloscope with its low channel count and high-speed sampling can still be used for serial interconnect debug in that it can show compliance to the specification eye diagrams. By its very nature, the oscilloscope can make the transition from parallel bus debug tool to serial interconnect debug tool, but what about the logic analyzer? The logic analyzer sampling time is not fast enough, and for protocol state analysis, there is no separate signal that can be used as the clock. For serial interconnects protocol analysis, engineers now have to choose between a new dedicated serial-interconnect-oriented tool or a new innovative add-on to their existing logic analyzer.

"The general purpose logic analyzer, when customized with analysis probes, lets users become familiar with one tool that is easily reconfigured for many different protocols and standards."

General purpose logic analyzer versus dedicated protocol analyzer

With the new Gbps serial interconnect standards, engineers must make some choices and accept some trade-offs when selecting validation and debug tools. One such choice is to select a *dedicated protocol analyzer,* or a general purpose *logic analyzer coupled with a serial interconnect analysis probe.*

A typical computer system employs multiple, different data bus and interconnect technologies, and each typically will require some debug and verification efforts. If one chooses dedicated protocol-analysis tools, then analyzing each bus or interconnect will require a different tool, each requiring a unique user interface to learn. Furthermore, acquiring a dedicated protocol analyzer for every interconnect implementation can add up to hundreds of thousands of dollars. When a particular technology inevitably is replaced by a newer one, the dedicated analyzer will be useless.

On the other hand, most digital designers already have made the financial and learning-curve investments in a general purpose logic analyzer. Using these with a single-instrument-based family of analysis probes, designers work with the familiar user interface for every protocol analyzer used.

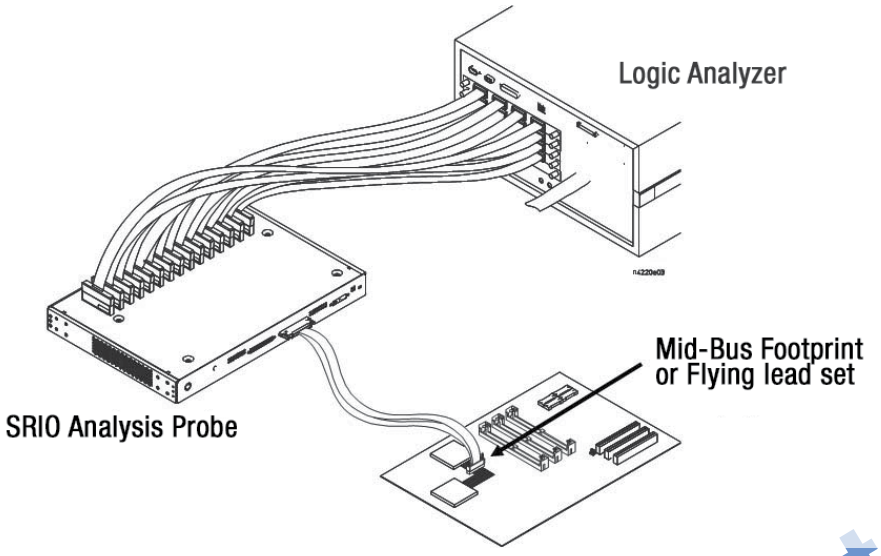


Figure 2

Logic analyzer offers the greatest measurement flexibility and versatility

To meet the challenges of design validation and test complexity that result from higher speeds and denser designs, Serial RapidIO designers need to look no further than their favorite logic analyzer vendor for a solution to these problems. Engineers have relied for decades on logic analyzers as an integral part of their validation and debug strategy. Analysis probes are essential to interface the logic analyzer with new, multigigabit (Gbps) architectures. Such probes sit between the target system and the logic analyzer, where they translate the high-speed serial interfaces into signals that can be processed by the logic analyzer (Figure 2).

On a single display, a single-instrument method offers the broadest spectrum of measurement capabilities, including cross-domain (simultaneous digital and analog) and cross-bus (simultaneous analysis of multiple protocols). Most analysis probes have software that facilitates inter-module collaboration, performs protocol decode, and simplifies triggering, store qualification, and performance monitoring of the device under test.

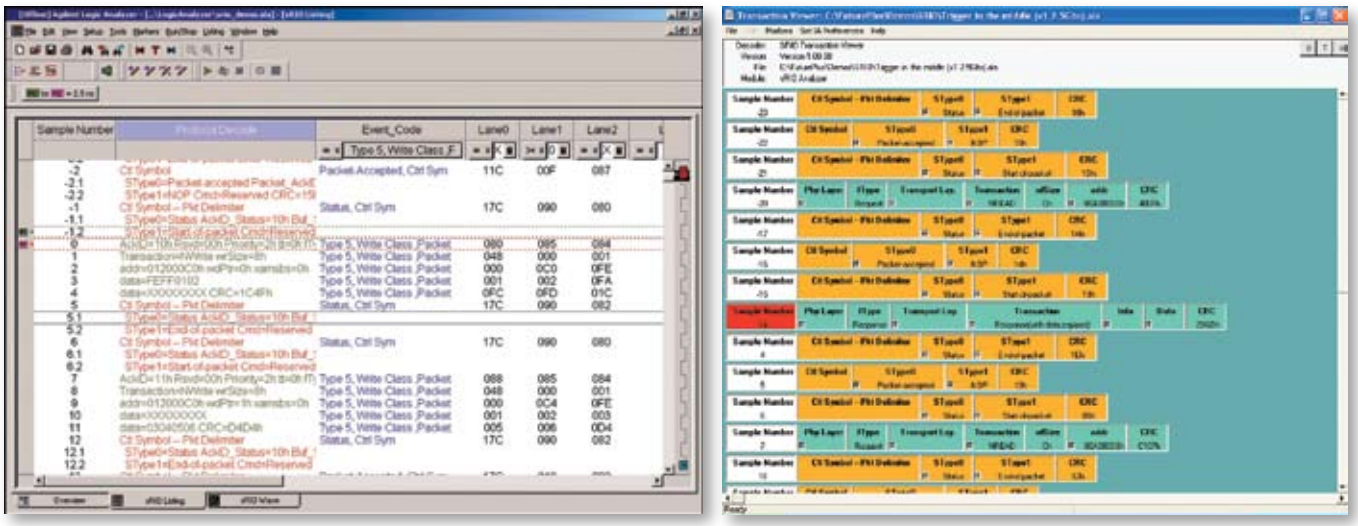
So the general purpose logic analyzer, when customized with analysis probes, lets users become familiar with one tool that is easily reconfigured for many different protocols and standards. Furthermore, the general purpose logic analyzer purchase can be more cost-effective across more designs due to this customization ease. The new GUI that now accompanies most analysis probes and logic analyzers makes combining tools seamless and easy to use.

Specialized serial analysis probes include software that runs on the logic analyzer to give the user a complete decode of the packet protocol traffic. There is no need to look at cryptic hex or binary characters. Analysis of SRIO can be done from a high-level graphical view or from a detailed text view (see Figures 3A and 3B, FuturePlus Systems FS4410 software).

Do I need to buy a new logic analyzer?

Existing logic analysis equipment can be used, at a substantial savings, to analyze modern interconnects including, for example, PCI-X, Serial RapidIO, PCI Express, and DDR.

For an up-to-date example, the FuturePlus FS4410 analysis probe can provide up to 3.125 Gbps Serial RapidIO analysis (Figure 4). Users who also are working with PCI Express applications can use the same probe and incorporate the SRIO performance with 2.5 Gbps PCI Express analysis for a substantially lower cost than would be incurred by acquiring a separate probe for each purpose. Each of these high-speed serial standards can be debugged using just two of the previous generation Agilent 16753 series of logic analysis cards, which will work in both



Figures 3A and 3B

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Bus	AT Expansion Bus			✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Universal Expansion Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓
	PCI Bus Masters	4	4	4	4	4	4	4	4	4	4		4	4
	APIC (add'l PCI interrupts)	9	9	9	9	9	9	9	9	9	9			
CPU and BIOS	CPU Max Clock Rate (MHz)	1400	1400	1400	1400	650	650	650	650	650	650	333	333	333
	L2 Cache	2MB	2MB	2MB	2MB	256k	256k	256k	256k	256k	256k	16K	16k	16k
	Intel SpeedStep Technology	✓	✓	✓	✓									
	ACPI Power Mgmt	2.0	2.0	2.0	2.0	1.0	1.0	1.0	1.0	1.0	1.0			
	Max Onboard DRAM (MB)	512	512	512	512	512	512	512	512	512	512	256	256	256
	RTD Enhanced Flash BIOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Nonvolatile Configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Quick Boot Option Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Boot	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
Peripherals	Watchdog Timer & RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	IDE and Floppy Controllers	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	SSD Socket, 32 DIP						1		1		1	1	1	
	ATA/IDE Disk Socket, 32 DIP	1	1	1	1	1		1		1				1
	Audio	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
	Digital Video	LVDS	LVDS	LVDS	LVDS			TTL	TTL	LVDS	LVDS	TTL	TTL	TTL
	Analog Video	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA
	AT Keyboard/Utility Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PS/2 Mouse	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Mouse/Keyboard	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O	RS-232/422/485 Ports	2	2	2	2	2	2	2	2	2	2	2	2	2
	USB 2.0 Ports	2	4	2	4									
	USB Ports					2	2	2	2	2	2	2	2	2
	10/100Base-T Ethernet	1		1		1	1	1	1	1	1	1	1	1
	ECP Parallel Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	aDIO(Advanced Digital I/O)	18	18	18	18	18	18	18	18	18	18	18	18	18
	multiPort(aDIO, ECP, FDC)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SW	ROM-DOS Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	DOS, Windows, Linux	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

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Bus	AT Expansion Bus	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Expansion Bus Master	✓	✓				✓							✓
	McBSP Serial Ports	✓	✓				✓							
Analog Input	Single-Ended Inputs	16	16	16	16	16	16							
	Differential Inputs	8	8		8	8	8							
	Max Throughput (kHz)	1250	1250	40	500	100	1250							
	Max Resolution (bits)	12	12	12	12	16	12							
	Input Ranges/Gains	3/7	3/7	3/1	3/4	1/4	3/6							
	Autonomous SmartCal	✓	✓											
	Data Marker Inputs	3	3		3		3							
Conversions	Channel-Gain Table	8k	8k		8k	8k	8k							
	Scan/Burst/Multi-Burst	✓	✓		✓	✓	✓							
	A/D FIFO Buffer	8k	8k		8k	8k	8k							
	Sample Counter	✓	✓		✓	✓	✓							
	DMA or PCI Bus Master	✓	✓		✓	✓	✓	✓						✓
	SyncBus	✓	✓				✓							
Digital I/O	Total Digital I/O	16	16	16	16	16	16	16	48	18/9	32	64	32	48
	Bit Programmable I/O	8	8		8	8	8	8	24	6/0				48
	Advanced Interrupts	2	2		2	2	2	2	2					2
	Input FIFO Buffer	8k	8k		8k	8k	8k							4M
	Opto-Isolated Inputs										16	48	16	
	Opto-Isolated Outputs										16	16		
	User Timer/Counters	3	3	3	2	3	3	3	3	3				10
	External Trigger	✓	✓		✓	✓	✓	✓	✓					✓
	Incr. Encoder/PWM									3/9				
	Relay Outputs												16	
Analog Out	Analog Outputs	2	2		2	2	2	4						
	Max Throughput (kHz)	200	200		200	100	200	200						
	Resolution (bits)	12	12		12	16	12	12						
	Output Ranges	4	4		3	1	4	4						
	D/A FIFO Buffer	8k	8k				8k	8k						

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Figure 4

the new 16900 and the earlier 16700 equipment frames.

Triggering and packet filtering

One new problem that serial interconnects pose is triggering and packet filtering. With parallel bus architectures, most of the triggering and filtering fell to the logic analyzer. However, since the logic analyzer is inherently a parallel machine, it does not have the "right stuff" to take on that job for the serial interconnect architectures. To overcome this constraint, triggering and packet filtering have become a key functionality of analysis probes. They must deserialize the data and provide a protocol-specific user interface that allows specifying the trigger and filtering.

In the triggering case, the hardware inside the analysis probe looks for the user-specified event and then sends the appropriate signals to the logic analyzer. The logic analyzer trigger menu can then perform a simple trigger or use more powerful triggering resources to look for more complicated events. Easy triggering for SRIO is shown in Figure 5.

Filtering is typically used to prevent transactions such as NOP, IDLE, or status information from ever being clocked into logic analyzer trace memory. Trace memory is costly, and any technique to use it more efficiently is well worth it. Filtering can also help remove unwanted traffic so that only the traffic of interest appears on the logic analyzer state-listing display. Powerful triggering and filtering improves the *time to insight* for design engineers using these tools.

How to connect

Up-front planning is advantageous to connect the analysis probe to the SRIO target. Connectorless probing is being adopted widely in order to nonintrusively probe 1.25 Gbps to 3.125 Gbps interfaces. The footprints or pads that are incorporated onto the PCB unit-under-test are standardized so that multiple vendors' test equipment can attach to them. This is a win for the industry, since engineers can design in one footprint at design time, and then pick the test equipment vendor when they are ready to test. In the past, the footprints were different between the vendors, so the design engineer had to make a commitment to a test vendor during design time. If that vendor delivered late or ended up not having the best equipment, the project team was in trouble.

For SRIO, the industry is using the same connectorless footprint that was used for the PCI Express industry. This allows design reuse and opens up the test equipment field to new players. This new style of connectorless probing includes a compression interconnect from the analysis probe to the target. The fact that there is no connector lowers the electrical loading of the analysis probe on the target. This leads to higher signal fidelity for the analysis probe and less electrical loading on the target. Figure 6, courtesy of Agilent Technologies, shows an example of a connectorless footprint and a compression probe.

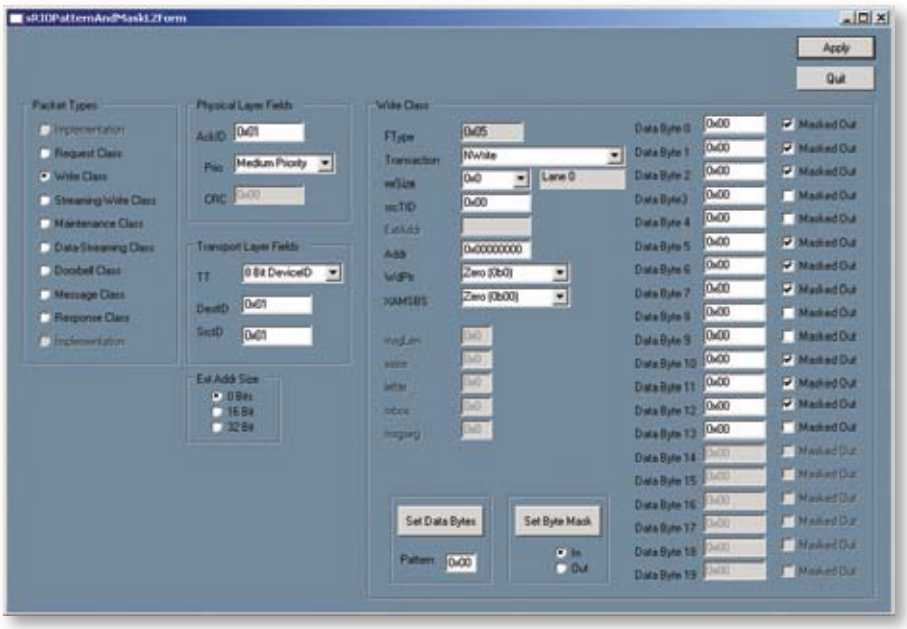

Figure 5

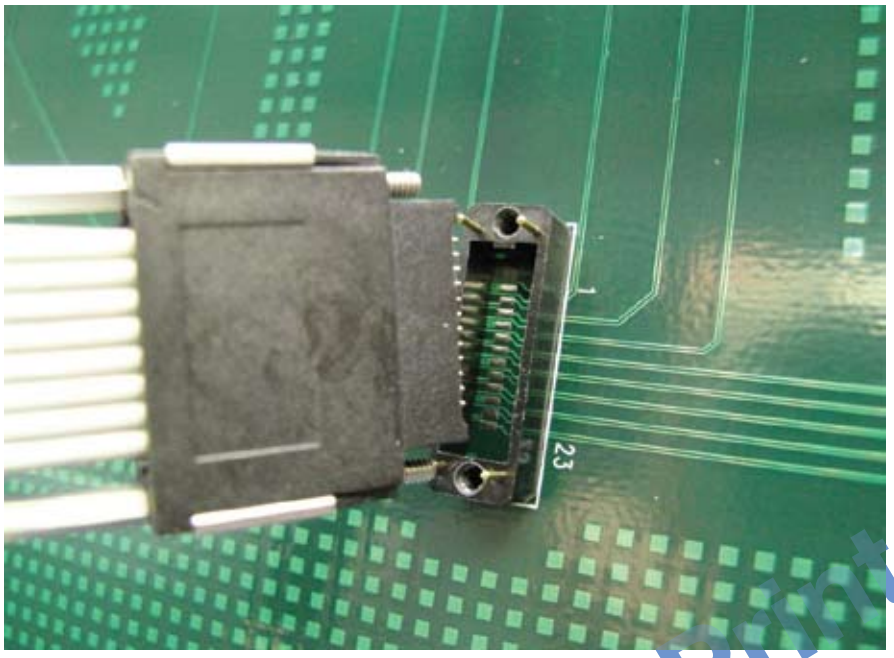

Figure 6

Since SRIO is a single lane or a four-lane, bidirectional link, all signals can fit on what is commonly known as the *half-sized footprint.* Complete details concerning the size of the footprint and pinout for SRIO can be found on the FuturePlus Systems website at: www.futureplus.com/download/appnotes/an_srio_fs4410.pdf.

Even though the SRIO footprint is small, there may not be enough room on some smaller and more densely packed designs for this footprint. Because of this constraint, some vendors now offer flying lead sets that are small and flexible.

Powerful, cost-effective solutions abound

Integrating Gbps interconnects in today's products need not compromise testing or break the capital equipment budget. High-performance and cost-effective tools are available to help design engineers tackle the most difficult test scenarios. Planning ahead for validation and debug is the key to successful product introduction. Engineers should team up with their favorite test-and-measurement vendor for the latest product information and design-for-test techniques so they can sail smoothly through the debug and validation phase of product development.

Barbara Aichinger *is vice president and cofounder of FuturePlus Systems. She has more than 20 years of experience with various bus and interconnect architectures and has spoken on test and measurement topics worldwide. Prior to founding FuturePlus in 1991, she was a principal engineer at Digital Equipment Corporation (DEC). At DEC, Barbara was the project engineer in charge of DEC's first RISC VMS-based machine. She was also DEC's representative to the IEEE for bus architectures and standards. Barbara holds a BSEE from the University of Akron, Ohio and an MSEE from the University of Massachusetts.*

For more information, contact Barbara at:

FuturePlus Systems
15 Constitution Drive
Bedford, NH 03110
Tel: 603-472-5905
E-mail: Barb.Aichinger@futureplus.com
Website: www.futureplus.com.

Multi-function radar systems for the deployed warrior using VPX-REDI and RapidIO

By James Meyer

Next-generation radar will need to provide enormous flexibility in terms of modes and functions. This application requirement will drive performance demands that have architectural implications for radar computing and electronics.

Photo courtesy of U.S. Navy

Advanced Multi-Function Radar (MFR) systems must simultaneously provide multimode search, multitarget tracking, Synthetic Aperture Radar (SAR) imaging, and Space Time Adaptive Processing (STAP). These systems will be deployed in some of the harshest and most demanding environmental conditions inside Unmanned Aerial Vehicles (UAVs), manned aircraft, and ship- and ground-based radar systems. The combined requirement of performance and ruggedization makes it challenging to service MFR applications using yesterday's Commercial Off-the-Shelf (COTS) technologies. However, COTS solutions based on open standards are now meeting the challenge of next-generation requirements. The combination of massive fabric bandwidth, Field Programmable Gate Array (FPGA) processing power, PowerPC high-compute density farms, and standards-based I/O housed in a conduction-cooled system address the simultaneous requirements of performance within an enclosure that can face the extremely hazardous field conditions found in deployed radar. VPX-REDI, a next-generation standard that combines the VITA 46 and VITA 48 standards (www.vita.com) with RapidIO (www.rapidio.org), significantly advances the robustness and performance of COTS sensor computing.

Challenges of mission-critical systems

Figure 1 shows an example flow of front-end data acquisition to back-end data processing and control. The challenge is to engineer and integrate highly reliable mission-critical systems that provide the deployed warrior with radar and navigation capabilities required for very challenging missions.

A typical leading-edge problem involves minimizing the enemy's broadband jamming efforts or eliminating ground or sea clutter located at arbitrary or unknown locations. The solution is to compute and track the angular locations of the jammers or clutter by appropriately processing the received signals and then adaptively generating a time-and-frequency-varying antenna pattern that places angular pattern nulls at the computed jammer location(s). Actual implementation depends upon a number of basic capabilities:

- Multielement antenna (8 to 100 elements)
- Separate receiver channel and A/D for each element/channel
- Efficient mapping of dedicated hardware for the pulse compression algorithms on FPGA modules
- Tightly coupled fabric connectivity for corner-turning operations
- Data exchanges with the high compute density processing modules for the final STAP and data processing

The I/O distribution for the STAP application described above entails more than 10 GBps of bisection bandwidth within a system and gigaflops of processing power. The two most challenging areas

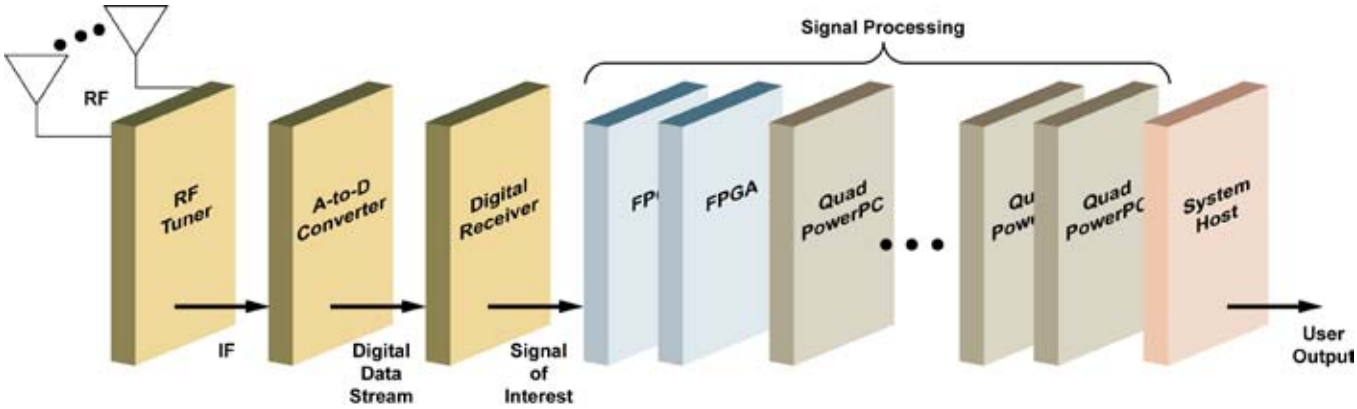

Figure 1

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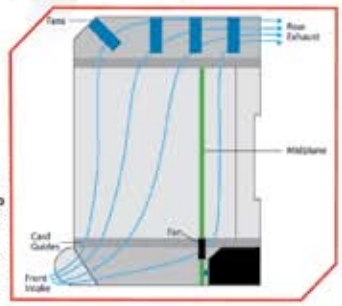

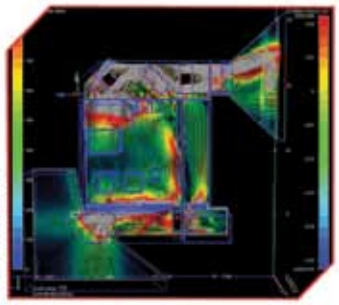

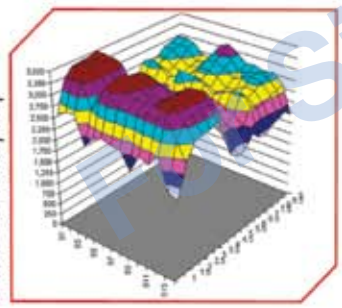

Hybrid Serial Parallel Cooling Delivers 99.999% High Availability

The Schroff Hybrid Serial-Parallel (HSP) cooling scheme uses axial fans in an innovative way to optimize shelf availability while minimizing downtime. Traditional fan trays contain rectangular combinations of serial and parallel fans with the goal of providing adequate bulk airflow to cool electronic components – at the design point. Fan failure conditions can compromise that ability, particularly in individual slots or regions.

Serial fan configurations, which boost air pressure, are subject to sharp pressure losses in the case of a fan failure. Such failures can cause power supplies and chips with high-fin-density heat sinks to overheat. Parallel fan arrangements push large volumes of air across multiple open surfaces – until a fan fails and recirculation occurs, substantially reducing the cooling to multiple slots.

Schroff's HSP design staggers the fans and arranges them at right-angles to the boards. The staggered fan distribution draws air from slots below and adjacent to each fan, but without the risk that a dedicated sealed channel presents. When a fan fails, the next fan upstream or downstream will continue to draw air with a marginally reduced cooling capacity until the fan is replaced. The end result is a dependable shelf with uniform slot-by-slot and front-to-rear airflow.

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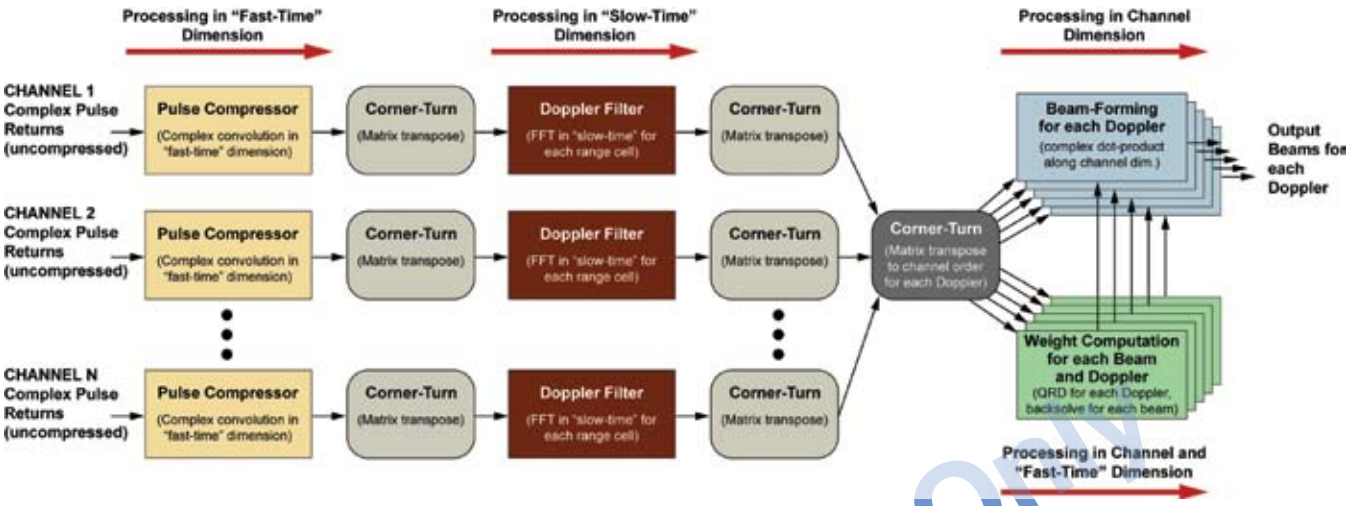

Figure 2

of the problem, shown in Figures 2 and 3, are the real-time receive beamforming computational rate at up to 40 MHz and the adaptive beam-forming weight computations at a rate of 100 Hz to 1,000 Hz.

Open standard COTS systems

By providing a modular COTS system based on open standards, the exceptionally demanding I/O in GBps and processing requirements of 10 to 100 GFLOPS for STAP and SAR algorithms can be met by combining the front-end functionality of high-speed microwave tuners and high-speed A/Ds in the speed range of 3 GHz or greater. Additionally, FPGAs and PowerPC resource modules are used for dedicated high-speed computations such as pulse compression operations for high-range resolution; effective short pulse response derived from the long, high-energy transmitted pulses; and lastly, returns. The complete processing chain operating on the three-dimensional (3D) radar data cube is shown in Figure 4.

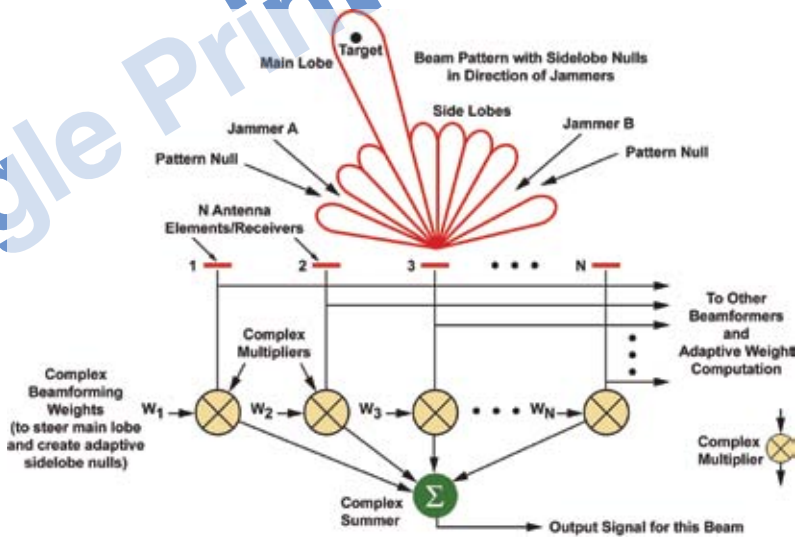

Figure 3

A system host carrier module(s) is needed to orchestrate and synchronize the radar receiver/exciter and data collection control and to prosecute the I/O distribution among the various FPGAs for signal conditioning and the general purpose processors for data processing and image formation. The switching fabric connects all of the modular components in the system facilitating the quick and efficient exchange of data between processors. This enables the implementation of corner-turning for the SAR algorithm at the maximum data rates of the packet switched Serial RapidIO fabric. The gold standard measure of fabric bandwidth in an all-to-all data exchange such as this one is bisection bandwidth. Bisection bandwidth measures the interconnect capacity between any randomly drawn halves of a topology. A RapidIO fabric in

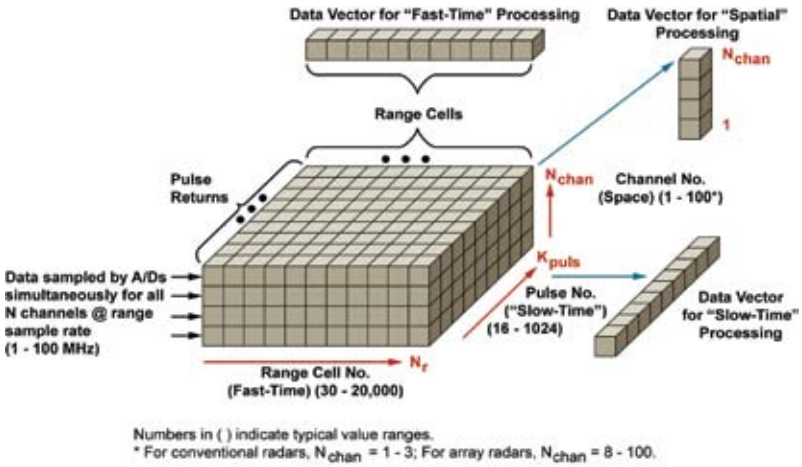

Figure 4

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a dual-star configuration can exceed 16 GBps of aggregate bisection bandwidth.

Algorithm challenges

To meet the grand algorithm challenges of today and tomorrow, such as the STAP spatial processing algorithm, a modular, hardware architecture – based on a new VITA standard form factor and switched I/O fabric – is required. The focus of the future STAP-capable radar system solution described later will be implemented using the larger 6U format of the VPX-REDI standard along with the Serial RapidIO switched fabric. The new system design, based on the new VPX-REDI form factor standard (VITA 46 and 48), provides the compute power and I/O bandwidth necessary to fully implement the STAP and SAR algorithms mentioned earlier. The PowerStream 6600 VPX-REDI rugged computer system from Mercury Computer Systems is an example of such a system. It can achieve more than 34 GBps of system-wide RapidIO fabric throughput. Its 16 modules can house 64 PowerPC processors or alternatively 21 user-programmable Xilinx Virtex-4 FPGAs. All this is accomplished in a conduction-cooled format made possible by the breakthrough VPX-REDI form factor.

The corner-turn (Figure 2) is one of the greatest challenges facing radar processing systems. VPX-REDI introduces a new module format based on a new set of high-speed differential signaling connectors. The adoption of a new connector set in the VPX-REDI standard paves the way for higher speed signaling, greater power budgets, and an enormous increase in I/O capabilities. VPX-REDI systems can achieve hundreds of GBps system throughput using high-speed serial fabric interconnects. One key difference in the architecture of VPX-REDI is its ability to support an expansive, full-mesh compute fabric topology through an increased number of serial fabric links on each module. The full mesh provides all-to-all connectivity without requiring that a slot be dedicated to fabric switching, as is the general case in other form factor architectures, namely VXS (VITA 41). There is also support for an interconnected common set of building block technologies including standard I/O mezzanine cards, PowerPC processors, FPGAs, and RapidIO fabric.

2 Level Maintenance

New radar systems require 2 Level Maintenance (2LM) where individual electronics modules are swapped out by the end user, literally in the field, when a failure occurs. VPX-REDI provides the electrical and mechanical infrastructure that protects individual electronics modules from static discharge (ESD) when they are being handled by ungrounded service personnel. This includes specially designed backplane connectors, carefully placed GND signals to sink excess current, and robust module covers.

Ruggedization

Mobile applications impose certain constraints on computing. Ground mobile vehicles can operate in regions of extreme temperature and in locations where the air is dusty or worse: chemically contaminated. This environment precludes the use of air convection cooling. Conduction cooling provides passive means by which heat can be conducted from the card to the outside wall of the chassis. The chassis wall can be cooled with a fan, but this has none of the implied problems of blowing air directly across the board. The conduction-cooling board exoskeleton also provides reinforcement for high-shock and vibration applications.

Airborne applications tend to prefer air cooling because it is lighter in terms of weight than conduction cooling. However, tactical fighters that achieve heights of 70,000 feet may have difficulty cooling electronics at low pressure. Despite its disadvantage of weight, these types of airborne applications also choose to make use of conduction cooling.

The solution

The radar compute subsystem that addresses the above-mentioned requirements comprises a VPX-REDI chassis and three basic processing modules that are connected via a Serial RapidIO backplane fabric and other backplane interconnects. The conduction-cooled modules in the system include an I/O mezzanine carrier, a PowerPC signal processing card, and an FPGA compute resource card. The VPX-REDI backplane provides a means for each slot to transfer data to any other of 16 slots via a RapidIO fabric interface without the use of a central switch card.

The I/O carrier module is a smart (processor-based) I/O mezzanine carrier that also serves as the scalar data and control processor for the radar receiver/exciter. It contains two MPC8548 processors that can serve as application processors or I/O engines servicing respective mezzanine card sites. The two mezzanine cards support PMC-X or XMC interfaces. This provides systems integrators with a wide and established ecosystem of option cards that may be incorporated.

The High-Compute-Density (HCD) module is a quad PowerPC AltiVec processor resource board. Each MPC7448 processor on the HDC operates at 1.4 GHz with a 400 MHz DDR2 memory interface. Each HCD module contains four PowerPC Compute Nodes (CNs) connected by a low-latency RapidIO crossbar to implement the network of fully connected floating point processors necessary to provide the GFLOPS of processing power for SAR and STAP algorithms.

The FPGA resource board houses three user-programmable Xilinx Virtex-4 FPGAs and can be delivered with an FPGA Developer's Kit (FDK). This kit puts the basic building blocks needed for system integration at the fingertips of developers: RapidIO fabric and Serial FPDP bridge end-point IP, data movement functionality, memory controllers, and so on.

A holistic solution for next-generation radar

Multi-function radar presents enormous challenges for system integrators, but COTS solutions based on open standards are now meeting them. The combination of massive fabric bandwidth, FPGA processing power, PowerPC high-compute density farms, and standards-based I/O is one important set of ingredients in challenging multi-function radar applications. The additional challenge is to house these features within a conduction-cooled enclosure that can face the extremely hazardous field conditions characteristic of field deployments.

James Meyer *is a senior systems applications engineer at Mercury Computer Systems. He is responsible for applying Mercury's high-performance multicomputer technology to customer projects including radar and sonar signal processing systems. Prior to joining Mercury, James worked at CSPI and Radix Systems on the development of noise abatement systems for submarines. He earned a Masters in Computer Science from Johns Hopkins University and a dual Bachelor's degree in Electrical Engineering and Bioengineering with honors from Syracuse University.*

To learn more, contact James at:

Mercury Computer Systems, Inc.
199 Riverneck Road
Chelmsford, MA 01824
Tel: 301-572-3012
E-mail: jmeyer@mc.com
Website: www.mc.com

The COTS software market doesn't run on DoD time

By Chris A. Ciufo

The U.S. military is long past the days of being able to design all of its software from scratch or mandate certain requirements that force COTS software companies to write code a certain way. One only has to look at defunct languages such as Forth or the barely commercially viable Ada environment to understand that the military has little or no clout with the COTS software industry. If Apple didn't bend to the pressure from the French government to open up its iTunes COTS software to non-iPod and non-Digital Rights Management (DRM) downloads[1] and if Microsoft can continue to drag its collective Windows feet in the face of European Commission threats, then the U.S. military doesn't have a prayer at influencing COTS software. The civilian collective markets of Europe are orders of magnitude larger than the DoD's consumption of COTS software.

Yet the DoD relies almost exclusively on COTS software in application form, as operating systems, development tools, or communications protocols. While the DoD *has* been successful at either creating or endorsing software standards such as DO-178B, ARINC-653, DoDAF, and DDS, COTS companies choose to follow these standards of their own free will because there's money to be made. In addition, these standards are either used by other customers besides the DoD – thus increasing the vendor's total available market and hence the possible upside return on investment – or the standards aren't much more than "military wrappers" put around an already in-use COTS software standard such as TCP/IP. Take a look at the DoD's mandate to use IPv6 (in lieu of IPV4) and it's obvious that only when the *entire Internet community* moves to IPv6 will the DoD meet its goal and stop issuing waivers for IPv6 nonconformance.

What the military needs to realize is how and why COTS software is created. Armed with this knowledge, specifiers and prime- and subcontractors will have an easier time mapping their COTS software requirements and expectations against what the open market is likely to do. In the accompanying article, *The emerging practice of software product line development* by Dr. Charles Krueger of BigLever Software, the author outlines the decision process that COTS software developers go through before bringing their products to market. Most importantly, he points out that software is rarely written as a stand-alone product anymore; instead, vendors create software *product lines* that are based upon predefined variations decided during development.

Charles offers some valuable insight into the four-step process used either consciously (or unknowingly) by COTS software companies. Understanding how COTS software is developed offers a valuable lesson that will aid program managers in specifying software, planning for tech refresh and code updates, and eventually dealing with preplanned obsolescence and possible porting to alternative platforms or software environments.

[1] *It has been widely rumored that Apple's counter to the French mandate was that the company would stop offering iTunes downloads to French IP addresses. With more than 80 percent market share in the portable music market, Apple probably had little to fear.*

The emerging practice of software product line development

By Charles W. Krueger, PhD

A new class of software development methods, tools, and techniques is emerging that greatly simplifies the engineering of product line portfolios. The improvements are so large that they impact the fundamentals of how companies do business.

In today's customer-driven environment, most companies target the needs of their prospective customers by creating a product line – a portfolio of closely related products with variations in features and functions – rather than just a single product. For example, a company that develops a radar countermeasures system will not be content selling that technology to just one client on one platform, but rather will see great economic benefit to engineering many variations of that product. Product variations could encompass different requirements for separate branches of the military, cockpit manufacturers, export rules and localizations for various countries, and a diversity of feature options and price points to support a wide range of anticipated and unanticipated customer requirements.

For companies that utilize embedded software in their products, this product diversity poses a serious problem. Tools and techniques for software development tend to focus on individual products. As a result, developing software for a *product line* is extremely complex due to multiple intertwined products, features, and production deadlines – all aimed at moving target markets. These tactical software development challenges are big enough to impede the realization of business-critical goals and strategies.

A new class of software development methods, tools, and techniques – collectively referred to as *software product line development* – is emerging to address this problem, offering improvements in development time to market, cost, quality, and portfolio scale and scope. What is most interesting is the *magnitude* of tactical and strategic improvements that are possible, not measured in percentage points but more commonly in factors of 2 to 10. These improvements are so large that they impact the fundamentals of how companies compete.

The genesis of software product line development methods

Manufacturers have long used analogous engineering techniques to create a product line of similar products using a common factory that assembles and configures parts designed to be reused across the varying products in the product line. For example, automotive manufacturers can now create thousands of unique variations of one car model using a single pool of carefully architected parts and one factory specifically designed to configure and assemble those parts.

> **"The idea of manufacturing software from reusable parts has been around for decades, but success has been elusive."**

The idea of manufacturing software from reusable parts has been around for decades, but success has been elusive. Recent advances in the software product line field have demonstrated that narrow and strategic application of these concepts can yield orders-of-magnitude improvements in software engineering capability. The result is often a discontinuous jump in competitive business advantage, similar to that seen when manufacturers adopt mass production and mass customization paradigms.

The characteristic that distinguishes software product lines from previous efforts is *predictive* versus *opportunistic* software reuse. Rather than put general software components into a library in

hopes that opportunities for reuse will arise, software product lines only call for software artifacts to be created when reuse is predicted in one or more products in a well-defined product line.

The concepts

Software product lines can be described in terms of four simple concepts, as illustrated in Figure 1:

- ***Software asset inputs:*** A collection of software assets – such as requirements, source code components, test cases, architecture, and documentation – that can be configured and composed in different ways to create all of the products in a product line. Each of the assets has a well-defined role within a common architecture for the product line. To accommodate variation among the products, some of the assets may be optional and some of the assets may have internal variation points that can be configured in different ways to provide different behavior.
- ***Decision model and product decisions:*** The decision model describes optional and variable features for the products in the product line. Each product in the product line is uniquely defined by its product decisions – choices for each of the optional and variable features in the decision model.
- ***Production mechanism and process:*** The means for composing and configuring products from the software asset inputs. Product decisions are used during production to determine which software asset inputs to use and how to configure the variation points within those assets.
- ***Software product outputs:*** The collection of all products that can be produced for the product line. The scope of the product line is determined by the set of software product outputs that can be produced from the software assets and decision model.

Software product line development approaches provide a shift in perspective so that development organizations can engineer their entire portfolio as though it were a single system rather than a multitude of products.

The benefits

The benefits of the software product line approach come in the form of tactical improvements in software engineering – deploying software products faster, cheaper, and better. However, what is most interesting is that these tactical improvements are often large enough to have an impact well beyond the borders of the

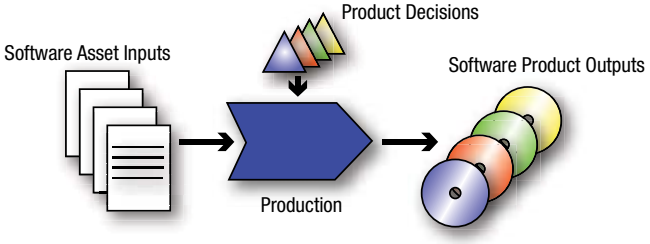


Figure 1

engineering department, offering strategic competitive benefits.

Time to market

If new products in a software product line are engineered and brought to market faster, strategic business benefits result. Companies with software product line success stories have reported decreasing their time to market for new products by factors of 2 to 50 when compared to the conventional techniques they were using.

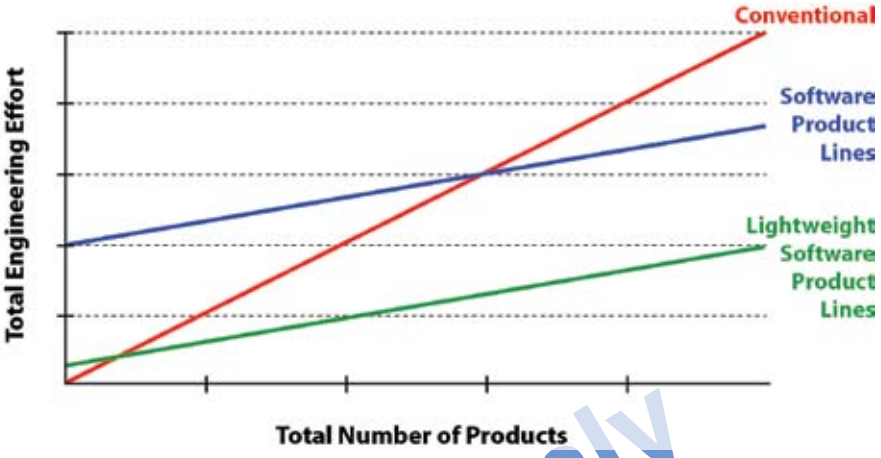


Figure 2

Quality

Quality benefits of software product lines can be measured in two ways. The first is how well each product matches the needs of each customer. The mass customization capabilities of software product lines directly address this measure of quality. The second is the rate of defects found in each of the products in the product line, which can also be significantly improved due to software reuse. Companies have reported reductions in defect rates as high as 96 percent.

Engineering cost

Software product line techniques can significantly increase the productivity of software engineers, seen as a reduction in the effort and cost required to develop, deploy, and maintain a portfolio. Typical productivity improvements reported in case studies range between a factor of 2 to 3, though higher factors are not uncommon.

Figure 2 illustrates the effort – and thus cost – required to develop, deploy, and maintain a portfolio. The red line represents a conventional productivity line. The blue line represents a productivity line of the pioneering efforts in software product lines, where a significant up-front effort was typically required (seen as the high Y-axis intercept) to launch a software product line. The green line represents the new generation of software product line methods that can achieve higher productivity gains with much less up-front effort.

Scalability

A company that takes a software product line approach needs to scale, without constraints, to whatever number of products is optimal for the business. The benefit of software product line approaches is that they can often scale to orders-of-magnitude more products in a portfolio than conventional software engineering techniques.

Advantages of software product line development

The emerging practice of software product line development offers significant tactical software engineering improvements as well as strategic business advantages. In much the same way that manufacturers advanced from manual labor to mass production to mass customization, software product line development allows software development organizations to advance from labor-intensive to highly efficient and automated portfolio development methods. To learn more about these methods and successes stories, see the community website www.SoftwareProductLines.com.

Charles W. Krueger, *PhD, is founder and CEO of BigLever Software and has 20 years of experience in software product line development. He has helped companies establish software product line practices, including* Software Product Line Hall of Fame *inductees Salion and LSI Logic. He is the author of more than 25 articles, including ACM* Software Reuse. *He is a frequent organizer and speaker for the International Software Product Line Conferences and moderates the community website SoftwareProductLines.com. He received his PhD in Computer Science from Carnegie Mellon University.*

To learn more, contact Charles at:

BigLever Software, Inc.
10500 Laurel Hill Cove
Austin, TX 78730
Tel: 512-426-2227
E-mail: ckrueger@biglever.com
Website: www.biglever.com

Editor's Choice Products

All-in-one SBC with cellular and ZigBee

In the industrial COTS world, the requirements for extended temperature and myriad connectivity apply equally well to military and defense applications. The LBC-GX500, an AMD Geode GX500 Pentium-class processor-based EBX board, specifically targets systems that need cellular, ZigBee, and multiple wired connections. Designed to operate at -40 °C to +85 °C, the board offers four wireless connections: Wi-Fi, GSM/GPRS cellular, CDMA cellular, and ZigBee RF. Not to rely solely on wireless, it also includes a 10/100 Ethernet port, six USB ports, six COM channels, a dial-up modem, and 48 parallel digital I/O lines.

The LBC-GX500 has everything you'd expect from a full-featured EBX-compliant SBC (5.75" x 8.0" or 146 mm x 203 mm), including CRT and LCD interfaces, keyboard/mouse, LPT parallel port, AC97 audio, and an optional 12-bit A/D. Disk drives (floppy, HDD, CompactFlash, and DiskOnChip) can be easily connected, and the board runs Windows CE, XP Embedded, Linux, VxWorks, QNX, and probably a few others. Amazingly, this all-in-one SBC consumes only about 8 W during normal operation and doesn't require a fan.

WinSystems
www.winsystems.com
RSC# 32072

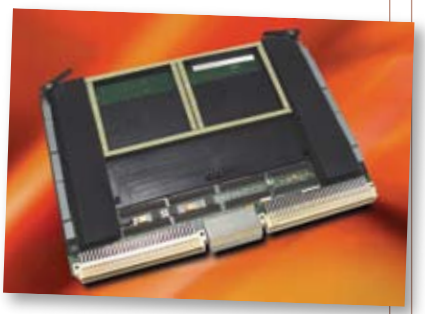
Rugged handheld ready for deployment

There are certainly rugged TabletPCs and laptops, and there are equally rugged PDAs. But like the Goldilocks children's fable, sometimes what's needed is a rugged handheld that's right in the middle. Enter the CATCHER by Catcher Holdings. The Communications And Telemetry Computing Handheld for Emergency Response (CATCHER) is specifically designed for military, government, and civilian first responders in emergency (or battlefield) deployments. Weighing just 2 pounds (or 3 pounds with two batteries), the MIL-STD-810F device can withstand 3-foot drops, up to 50 *g*s, and is weather resistant.

Based on an Intel Pentium M with 2 GB of DRAM and a 40 GB HDD, the unit runs a Windows XP OS featuring pen computing extensions and offers Wi-Fi, Bluetooth, GPS, and optional CDMA, GSM/GPRS, and UWB cellular connectivity. Multimedia is supported with hardware codecs, and the CATCHER comes complete with stereo speakers and a microphone. The 850 nit backlit 6.4" VGA display is intended to be used in full sun. Onboard sensors include a fingerprint reader and UPC barcode reader, and the CATCHER can be outfitted with an optional RFID interrogator/reader to aid in inventory (or human) tracking.

Catcher Inc.
www.catcherinc.com
RSC# 32086

Two many: Each is independent

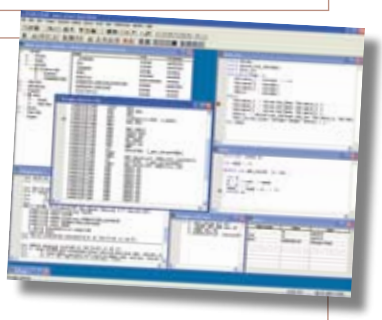


You'll find lots of dual-CPU SBCs in the market, though requiring conduction cooling admittedly narrows the search quite a bit. Still, when ultimate performance is a requirement, it's better to have dual processor subsystems – just like the C102 from Aitech does. This MPC7448-based SBC uses two 1.42 GHz CPUs, each with its own 1 GB of ECC SDRAM @ 166 MHz, 12 MB of boot flash, 256 MB of user flash, and 128 kB of NVRAM. The nodes are interconnected via PCI-X at 133 MHz, and I/O from the PCI-PCI bridge can also be fed to the VME backplane at up to 2eSST (320 MBps) speeds.

In addition, there are four Ethernet ports (two 10/100/100 and two 10/100), two USB 2.0 ports, a Serial ATA port, six USART ports, two UART ports, and 16 TTL/eight differential lines. The board can accommodate two PMC modules but already includes two dual redundant MIL-STD-1553 ports on the basecard. Of course, since this board is designed for harsh military environments, there are the requisite features such as BIT and IBIT, along with various onboard monitor/debugger utilities.

Aitech
www.rugged.com
RSC# 31018

Ada for real-time Windows



RTX is a low-footprint (250 kB of RAM), high-performance extension to Windows that allows apps to run in real time with features like preemptive scheduling. If you happen to be running Ardence's RTX, you're probably doing it with C/C++. But suppose you could run Ada. Would this make RTX more appealing for an embedded military environment? DDC-I thinks so. They've introduced the SCORE IDE for RTX version 6.x, which promises a mixed Ada/C/Embedded C++ environment – all in a deterministic Windows framework where Ada tasks run as RTX threads.

SCORE is a multilanguage, object-oriented IDE for developing and deploying safety-critical applications. It includes optimizing compilers for Ada, C, Embedded C++, and Fortran 77. The GUI-based tool includes source editor, project manager, and automated build/make utilities. It also has a multifunction debugger to make life easier with respect to syntax, expressions, stacks, and other code "gotchas." SCORE can debug RTX applications running in both the Win32 and RTSS environments, and it can be runtime certifiable to DO-178B.

DDC-I
www.ddci.com
RSC# 32087

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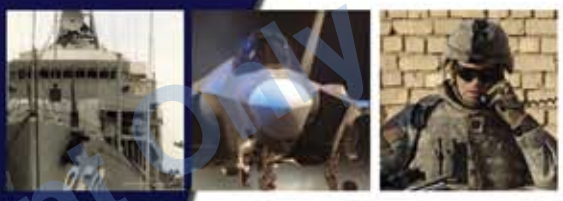

Supporting
Homeland Security

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Product Guide:
XMC base boards, mezzanine boards, and related XMC products

Vendor	Model number	Description	Form factor	# XMC sites
Base boards				
Kontron www.kontron.com	CP6012	A server-class 6U CompactPCI processor blade with Intel's Core Duo processor T2500 at 2 GHz, E7520 chipset, and 6300ESB I/O hub • Up to 4 GB dual-channel DDR2-SDRAM @ 400 MHz, ECC, SODIMM socketed • Four GbE ports (82571EB), two front/two rear/PICMG 2.16, four USB 2.0, two Serial ATA, onboard HDD or CF • Legacy I/O: Two COM RS-232/422/485, floppy, IDE, PS/2 (rear only) • XMC (x4 PCIe)/PMC (PCI-X) expansion site, 64-bit/66 MHz CompactPCI interface, 3.3 V/5 V support	6U CompactPCI	1
Innovative Integration www.innovative-dsp.com	PMC/XMC FPGA Cards	Velocia PMC/XMC family integrates ultra-fast signal capture, generation, and co-processing on an advanced PMC architecture • Virtex-II Pro FPGA • 64/66 PCI with a private JN4 64-bit user I/O port • XMC four-lane Rocket I/O (per VITA 42) • Allows for rapid deployment of SDR, signal intelligence, radar, and radio test equipment • Includes SIO module, dual 1 Gbps Tx/Rx Serial I/O ports, DR module 16-channel digital receiver card,UWB ultra-wide digital receiver, and TX digital transmitter	PMC/XMC	1
CES www.ces.ch	RIO4 8076	A ruggedized conduction-cooled reconfigurable PowerPC-based 6U VME 2eSST computer • Single or dual computing node, each node equipped with: PowerPC G4 at maximum available frequency; Virtex-II Pro FPGA with a private ultra-high-speed SSRAM; high-speed communication channels • Two GbE channels • One PMC site with a Rocket I/O interface • VME64x 2eSST and two separate PCIs (local/P0) for transparent multiprocessor extension • 16-channel concurrent chained DMA logic • Four high-speed interprocessor serial links on backplane and PMC site (XMC standard)	6U VME	2
Radstone Embedded Computing www.radstone.com	V4DSP	Dual Virtex-4 FX FPGA processor with MPC7448 GPP node • 2x Virtex-4 processing nodes: XC4VFX60 or XC4VFX100 • 1x MPC7448 general purpose processing node at 1-1.4 GHz • 1x PMC/XMC site • 2x StarFabric ports to P0 for expandability • 2x 2.5 GHz MGTs to P0 for high-speed Serial I/O • VxWorks BSP support, V-Wrap FPGA wrapper support with VHDL source and documentation, AXIS support • Air- and conduction-cooled • Support for ICS-8550 ADC XMC	6U VME	1
Concurrent Technologies www.gocct.com	VX 405/04x SBC	The VME/VXS SBC supports Intel Core Duo processors and can be used in VME64x or VXS 41.3 backplanes • Single slot high-performance VME64x/VXS SBC • 2.0 GHz or 1.66 GHz Intel Core Duo processor with 667 MHz FSB • Utilizes the Mobile Intel 945GM Express chipset with ICH7-M I/O hub • Up to 4 GB of 667 MHz DDR2 SDRAM • 32/64-bit PMC module interface, operating at 33/66 MHz • XMC module interface • Extended temperature version available: -25 °C to +70 °C (E-Series), -40 °C to +55 °C (J-Series), supporting 1.66 GHz processor	6U VME or VXS VME	1
Curtiss-Wright Embedded www.cwcembedded.com	CHAMP-AV6	VPX Quad PowerPC 8641 • Quad PowerPC 8641/8641D processors at up to 1.33 GHz • Up to 1 GB DDR2 SDRAM with ECC per processor • Each processor has dual 64-bit memory banks • VPX-REDI format (1 " pitch) with four Serial RapidIO ports on P1 connector and option for one PCI Express port • 512 MB flash with write-protection • 128 kB NVRAM • One XMC site supporting PCI Express • Curtiss-Wright Controls Embedded Computing's Linux 2.6 SDK • Designed for military harsh-environment applications • Air- and conduction-cooled available	6U VPX VME	1

Vendor	Model number	Description	Form factor	# XMC sites
Curtiss-Wright Embedded www.cwcembedded.com	VPX6-185 Dual PowerPC 8641	A general purpose SBC with Freescale 8641 PowerPC processor • Single or dual processor e600 cores at up to 1.33GHz • Up to 2 GB DDR2 SDRAM controlled by dual 64-bit controllers • Two PMC/XMC sites supporting parallel PCI and PCI Express • VPX/VPX-REDI formats with four Advanced Switching Interconnect (ASI) switch ports on P1 connector and option for one Serial RapidIO port • Continuum Software Architecture (CSA) firmware providing a comprehensive suite of system debug, exerciser, and update functions, BIT, and nonvolatile memory sanitization function • Air- and conduction-cooled versions	6U VPX VME	2
Micro Memory www.micromemory.com	MM-1600	A quad FPGA VPX VITA 46 carrier with two PMC/XMC sites and four Serial RapidIO ports on P1 • Targets streaming signal sensor applications such as synthetic aperture and phased array radar, signal intelligence, and Software-Defined Radio • Primary DDR capacity: 2 GB • CoSine primary device: 2VP70 • CoSine companion device: SX55 • Format: VITA 41	6U VPX VME	2
Micro Memory www.micromemory.com	MM-1650	A quad FPGA VPX VITA 46 carrier with two PMC/XMC sites and four Serial RapidIO ports on P1 • Targets streaming signal sensor applications such as synthetic aperture and phased array radar, signal intelligence, and Software-Defined Radio • Primary DDR capacity: 2 GB • CoSine primary device: 2VP70 • CoSine companion device: LX160 • Format: VITA 46	6U VPX VME	2
Micro Memory www.micromemory.com	MM-1550	A quad FPGA VXS VITA 41 carrier with two PMC/XMC sites and two Serial RapidIO ports on P0 • Targets streaming signal sensor applications such as synthetic aperture and phased array radar, signal intelligence, and Software-Defined Radio • Primary DDR capacity: 2 GB • CoSine primary device: 2VP70 • CoSine companion device: LX160 • Format: VITA 46	6U VXS VME	2
VMETRO www.vmetro.com	Phoenix M6000	A VXS I/O controller with dual XMC/PMC sites and dual 4 Gbps Fibre Channel • Dual XMC sites with x8 PCI Express connections • VXS interface implemented using Virtex-4 FX FPGA • AMCC PowerPC 440SP processor • Dual 4 Gbps Fibre Channel ports • 320 MBps 2eSST VME interface • 256 (512) MB high-speed streaming memory • Onboard PCI Express switch for optimal data flow • Independent 64-bit, 133 MHz PCI-X bus for each PMC site • Ruggedized versions available	6U VXS VME	2
VMETRO www.vmetro.com	Phoenix VXS Systems	Systems built around high-performance processing, I/O, and multichannel Gbps serial communications with supporting software and firmware • High-performance data processing utilizing dual PowerPC and dual FPGA CPUs • High-speed communications through a VXS fabric, multichannel data links, and raw or switch-packet protocols • High-speed serial communication, zero-latency switch cards • Intelligent PMC/XMC I/O controller, carrier, and recorder blade • TransComm FPGA Communications Toolbox for low-latency, efficient data communications	6U VXS VME	1
Micro Memory www.micromemory.com	MM-1500	A VME board that includes the V-4TM SXTM series of FPGAs from Xilinx • Targets streaming signal sensor applications such as synthetic aperture and phased array radar, signal intelligence, Software-Defined Radio, and semiconductor and medical imaging • Primary DDR capacity: 2 GB • CoSine primary device: 2VP70 • CoSine companion device: SX55 • VITA 41 format	VME	2

Vendor	Model number	Description	Form factor
XMC mezzanine boards			
Curtiss-Wright Embedded www.cwcembedded.com	RazorBlade III-SX & IV-LX	Optical fiber XMC modules • Deliver 24 ports of wire-speed GbE performance over copper and optical fiber when used with the SVME/DMV-680 SwitchBlade GbE switch • Provide a powerful building block that can be used to design Intra-Platform Networks (IPN) that link IP-based networks onboard air, land, and sea vehicles in defense and aerospace applications • Suitable for applications where high signal quality, secure data transmission, and survivability are essential	XMC
Radstone www.ics-ltd.com	ICS-8550	An XMC module designed to bring more bandwidth and processing power to Software-Defined Radio applications • Features two analog inputs equipped with AD9430 210 MHz, 12-bit ADCs, and a Xilinx Virtex-4 XC4VFX60 FPGA • Optimized for wide bandwidth front-end digital signal processing for digital receiver applications in signal intelligence and radar systems • Five levels of ruggedization available	XMC
VMETRO www.vmetro.com	SFM Quad Serial FPDP Module	A high-performance PMC/XMC module • Supports up to four simultaneous Serial FPDP (VITA 17.1-2003) channels • Provides a higher level of functional density without creating a bottleneck getting the data to and from the baseboard • Separate DMA controllers for each channel • Supports PCI-X data transfers at speeds up to 133 MHz • Supports PCI Express via the XMC connectors and provides the full 2.5 Gbps data rate per channel • One, two, or four Serial FPDP channels • 1.0625, 2.125, and 2.5 Gbps PCI Express link speed per channel in XMC form factor • 64 Mb FIFO per channel with programmable elasticity • VxWorks and Linux support	XMC
Pentek www.pentek.com	Model 7142	Transceiver module • Four-channel A/D, one-channel D/A with Virtex-4 FPGAs • Four 125 MHz 14-bit A/Ds • Conduction-cooled and ruggedized versions • Complete software radio interface solution • VITA 42.0 XMC compatible with switched fabric interfaces • One digital upconverter • One 500 MHz 16-bit D/A • 768 MB of DDR2 SDRAM • 32 pairs of LVDS connections to the Virtex-4 FPGA for custom I/O on P4	XMC, 3U/6U CompactPCI, PCI
Pentek www.pentek.com	7140 Transceiver	A dual digital up/downconverter PMC/XMC with FPGA • VITA 42.0 XMC compatible with switched fabric interfaces • Two 105 MHz 14-bit A/Ds and four digital downconverters • One digital upconverter and two 500 MHz 16-bit D/As • 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O on P4 • 512 MB of DDR SDRAM • Up to 2.56 seconds of delayer data capture at 100 MHz • Ruggedized and conduction-cooled versions available • Available in 3U and 6U CompactPCI and PCI formats • PCI format SCA compliant	XMC/PMC, 3U/6U Compact PCI/PCI
Pentek www.pentek.com	Model 7140	A dual digital up/downconverter PMC/XMC with FPGA • Complete software radio transceiver solution • Ruggedized and conduction-cooled versions available • VITA 42.0 XMC compatible with switched fabric interfaces • Two 105 MHz 14-bit A/Ds • Four digital downconverters • One digital upconverter • Two 500 MHz 16-bit D/As • 512 MB of DDR SDRAM • Xilinx Virtex-II Pro FPGA • Up to 2.56 seconds of delay or data capture at 100 MHz • 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O on P4	XMC/PMC, CompactPCI, PCI
ACT/Technico www.acttechnico.com	8753	A PrPMC/XMC mezzanine card based on Freescale's MPC7447A or MPC7448 processor • Can be used in conjunction with VME or CompactPCI carriers or with proprietary designs • 64-128 MB soldered MirrorFlash; 2 MB high-speed SRAM; 32 kB SPI EEPROM; and 2 kB I2C EPROM • Dual PMC/XMC VME64x carrier with VME2eSST capabilities	XMC/PrPMC

Vendor	Model number	Description	Form factor
Pentek www.pentek.com	Model 7142	Transceiver module • Four-channel A/D, one-channel D/A with Virtex-4 FPGAs • Four 125 MHz 14-bit A/Ds • Conduction-cooled and ruggedized versions • Complete software radio interface solution • VITA 42.0 XMC compatible with switched fabric interfaces • One digital upconverter • One 500 MHz 16-bit D/A • 768 MB of DDR2 SDRAM • 32 pairs of LVDS connections to the Virtex-4 FPGA for custom I/O on P4	XMC, 3U/6U CompactPCI, PCI
Other, XMC-related			
VMETRO www.vmetro.com	VanguardExpress XMC	PCI Express protocol and link analyzer for XMC form factor • Support for x1 to x8 PCI Express • Analyzer, statistics, and protocol checker operate independently and concurrently • 256 MB trace buffer • Ethernet or USB host connection • Arrange trace data in packet, link, split transaction, data, or lane views • Stackable architecture to carry a XMC under test • Temperature and voltage monitor • Real-time performance monitoring for predefined and user-defined events • Automatic detection of PCI Express protocol errors	Test equipment

Data was extracted from OSP's product database on Oct. 18, 2006. Search criteria included the category "Mezzanine: XMC," description keyword "XMC," and the XMC form factor checkbox on products entered 10/1/05 through search date within *VMEbus Systems, Military Embedded Systems, PC/104 and Small Form Factors,* and *DSP-FPGA.com* magazines. Entries were further edited for relevance to product guide's theme. OpenSystems Publishing is not responsible for errors or omissions, and vendors are encouraged to add their new products to our website at www.opensystems-publishing.com/vendors/submissions/np/

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New Products

www.mil-embedded.com/rsc

By Sharon Schnakenburg

BRIDGE: cPCI-to-cPCI Express

One Stop Systems Inc.
Website: www.onestopsystems.com
Model: OSS-HYB-3U/6U RSC No: 30583

Hybrid bridge board that bridges between CompactPCI Express slots and CompactPCI slots in a single backplane when plugged into a hybrid bridge slot • 3U or 6U connectors • Requires hybrid slot on backplane

CARRIER BOARD: PMC

Dynamic Engineering
Website: www.dyneng.com
Model: cPCIBPMC3U64ET RSC No: 31459

CompactPCI-to-PMC adapter/carrier converter card • Suitable for putting extended temperature PMCs into CompactPCI environments • Easy to use with a plug-and-play interface to the PMC • 3U 4HP CompactPCI • 1 PMC slot provided • CompactPCI bus can operate at 66 or 33 MHz • 64- or 32-bit operation supported • Extended temperature range of -40 °C to +85 °C • Conformal coating optional • Software interface: PMC register definitions as defined by installed hardware; no software setup required • Power: +5 V, +3.3 V, +12 V, -12 V, and VIO supplied to PMC

Radstone Embedded Computing
Website: www.radstone.com
Model: ICS-8500 RSC No: 31430

Rugged FPDP/FPDPII receiver/transmitter PMC • 8 MB buffer memory • FPDP I/O via PMC P4 connector • PCI 2.2 64-bit, 66 MHz PCI interface • FPDPII 400 MBps interface • Software-controlled channel selection and corner-turning capabilities • Windows, Linux, and VxWorks device drivers

COUNTER/TIMER

ACCES I/O Products, Inc.
Website: www.accesio.com
Model: USB-CTR-15 RSC No: 31344

USB/104 digital module that provides 15 independent counter/timers • High-speed USB 2.0 device, USB 1.1 compatible • 15 independent 16-bit counter/timers (5x 82C54-10) • Clock, gate, and output signals from all 15 channels buffered and accessed via one connector • PC/104 module size (3.550" x 3.775") and mounting compatibility • Standard configuration adapter preconfigured for event counting, frequency measurement, pulse width measurement, or frequency generation • User wiring adapter card provided for flexible yet easy counter concatenation/configuration • Rugged, small-sized (4" x 4" x 1.25") steel industrial enclosure • OEM (board only) version available

DATA ACQUISITION

Micro Memory LLC
Website: www.micromemory.com
Model: Anvil RSC No: 31361

A storage subsystem that provides an all-digital front-end solution to data recording • Enables the use of hierarchal storage and supports high sustained front-end throughput • Large density, low-cost SATA hard disk drives can be reliably utilized for secondary storage where SCSI or fibre channel drives would otherwise be required • Native PowerPC and GbE with optional support for x86 processor platforms (via PrPMC site) • Ideally suited for acquisition of real-time sensor data for recording or signal analysis in applications such as radar, signal intelligence, Software-Defined Radio, and telemetry • Includes up to 64 GB of high throughput, dual access SDRAM memory • Four full-length, full-height PCI slots accommodate a variety of sensor input I/O – A/D, Serial FPDP, and custom LVDS or fiber links – plus storage output I/O for Fibre Channel, SCSI, or SATA • Fewer hard disk drives can be utilized to achieve bandwidth and storage requirements

FIELDBUS: PROFIBUS

Mesa Electronics
Website: www.mesanet.com
Model: 5I21 - FPGA BASED RSC No: 31102

A programmable serial interface card for the PCI bus • Supports up to 12 full duplex RS-422 or half duplex RS-485 serial links with baud rates up to 10 Mbaud • Uses a 400 K gate Spartan-3 FPGA and a bus mastering PCI bridge for high performance • The I/O connector is a 68-pin high-density type compatible with standard 100 ohm differential cables • Suitable for high-speed motion control systems, industrial I/O, custom real-time distributed I/O, supporting legacy hardware, and almost any high-speed serial interface application that requires a flexible, high-performance, universal serial interface card

I/O: FPGA

VMETRO
Website: www.vmetro.com
Model: DEV-FPGA05D RSC No: 30635

A Xilinx Virtex-5 XC5VLX50 platform FPGA-based, short PCI card with high-speed digital I/O and PCI-X interface to the host computer • Aimed at application development • Xilinx Virtex-5 LX50 FPGA • Multiple banks of memory for demanding DSP • I/O adapter modules to support external interfaces (includes LVDS, RS-422, Cameralink) • Windows support

I/O: INDUSTRIAL

Samtec
Website: www.samtec.com
Model: Acclimate RSC No: 30762

IP68 sealed circular I/O interfaces for rugged/harsh environment applications • Meet IP68 specifications for dust and waterproof sealing in industrial or other rugged/harsh environment applications • Includes interfaces for Ethernet (SCRE/SCPE Series) and USB (SCRU/SCPU Series) applications • Both ends of the system are offered with standard cable plugs available up to 2 meters in length • The USB system can be specified with either A Type or B Type plugs on either end

I/O: MULTIFUNCTION

North Atlantic Industries
Website: www.naii.com
Model: 73LD4 RSC No: 31642

A six-channel LVDT/RVDT-to-digital converter on a PC/104 card • DSP-based 73LD4 includes six independent, transformer isolated, programmable LVDT/RVDT tracking converters • 16-bit resolution, ±0.025% F.S. accuracy • Accurate digital velocity output, incremental encoder (A+B) outputs • Wrap-around self-test • Frequency range of 360 Hz to 10 kHz

Pentek, Inc.
Website: www.pentek.com
Model: Model 6821-422 RSC No: 31914

GateFlow 215 MHz A/D and digital receiver - VME • FPGA installed core VME board • AD9430 12-bit 215 MHz A/D converter • Dual GateFlow Core 422 296 MHz wideband DDCs, factory-installed • Xilinx Virtex-II Pro FPGAs • Four sets of 18-bit user programmable FIR filter coefficients • Four FPDP or FPDPII front panel outputs • FIFO buffering for real-time recording • Ruggedized and conduction-cooled versions available

MASS STORAGE: PLUG-IN UNIT

WinSystems, Inc.
Website: www.winsystems.com
Model: 8GB CompactFlash RSC No: 31927

An 8 GB CompactFlash card • -40 °C to +85 °C temperature operation fills storage needs in rugged application environments • CompactFlash card densities: 8 GB, 4 GB, 2 GB, 1 GB, 512 MB, 256 MB, and 128 MB • 32-bit RISC controller • Fixed disk operation and true IDE mode capable • Unlimited reads and 10-year data retention • Low power consumption • -40 °C to +85 °C operating temperature

MASS STORAGE: SOLID-STATE DISK

General Micro Systems, Inc.
Website: www.gms4vme.com
Model: "Index" VCNAS RSC No: 31529

Conduction-cooled Network Attached Storage (NAS) system for severe environments • Onboard high-performance 1.4 GHz Pentium M CPU • Up to 2 GB of 266 MHz DDR SDRAM with ECC for data buffering • Supports up to 200 GB of rotating media, or for the most secure or severe applications, up to 128 GB of flash drive in a single slot (4HP) VME form factor • Ultra-small footprint, 6U, 4HP (single slot) • Compliant to IEEE Std. 1101.2 and ANSI/VITA 20-2001 • Ultra-low power requirements: 16 W average • Smart Write algorithm to extended flash life cycle • Dual GbE ports, support fiber to front panel, or

VITA 31.1 • TCP/IP Offloading Engine (TOE) on both GbE ports • NAS capacity may be extended by daisy-chaining via Ethernet ports • Allows multiple CPU boards with different OS to boot from one NAS unit • Two NAS units may be used to mirror each other for redundant data • Supports HTTP, FTP, TFTP, TELNET, and NFS servers • Support for NFS, FTP, and TELNET client sessions • VME64 support via Tundra Universe II (optional) • Rugged extended temperature range of -40 °C to +85 °C

MEZZANINE: CCPMC

Aitech Defense Systems
Website: www.rugged.com
Model: M222 RSC No: 31438

A rugged/mil spec, high-density, NAND flash-based PMC mass memory module • Up to 64 GB NAND flash memory in two banks • >45 MBps transfer rate (sustained) • Low power consumption <4 W • PCI Rev. 2.3 compliant supporting 64-bit @ 66 MHz • VxWorks and LynxOS RTOS support with Flash Low Level (FLL) driver • Optional Flash Memory Manager (FMM) for auto wear-leveling, bad block mapping, and so on • Full file system read/write emulation • IEEE 1386-2001 (air-cooled) or VITA 20-2001 (conduction-cooled) • Commercial/military level ruggedization • Vibration and shock resistant

PROCESSOR: CELERON M

BCM Advanced Research
Website: www.BCMCOM.com
Model: EBC5852-C8 RSC No: 31137

RoHS (lead-free) 5.25" SBC • Operates with a single DC +12 V input • Based on the Intel 82852GM GMCH and 82801DB ICH4 chipset architectures • Supports Intel Celeron M processor in onboard BGA format • Runs with a 400 MHz FSB and has one 200-pin DDR SODIMM socket that will support up to 1 GB PC2100 non-ECC system memory • Features an 18-bit dual channel LVDS output for LCD panels, one IDE connector, two SATA connectors, and a CompactFlash socket • Features additional I/O including two serial ports, six USB 2.0 ports, one 10/100 Mbps LAN, one GbE interface, and one 32-bit PCI slot • Thermal sensor for hardware monitoring capabilities • Supports the ACPI V2.0 specification • For any application that requires a small footprint, high-performance solution

PROCESSOR: PENTIUM M

Fastwel
Website: www.fastwel.com
Model: Fastwel CPC1700 RSC No: 31632

A PC/104-Express format single board computer designed for mission-critical embedded systems • Intel Pentium M processor up to 2.26 GHz and 533 MHz FSB • 1 GB PC4200 DDR2 SDRAM soldered onboard • Four x1 PCI Express expansion interfaces • Two GbE ports • Two independent CRT/LVDS displays • Two Serial ATA channels • Operating temperature: -40 °C to +85 °C

MEN Micro Elektronik GmbH
Website: www.menmicro.com
Model: D601 RSC No: 31924

A conduction-cooled 6U CompactPCI Pentium M SBC • Fanless operation in military, aerospace, and industrial control applications • With either the 1.4 GHz Low Voltage (LV) Pentium M or the 1 GHz Ultra-Low Voltage (ULV) Celeron processors, a temperature range of -40 °C to +85 °C is supported • Can be equipped with Intel processors with speeds up to 2 GHz • 32-bit/33 MHz interface to the CompactPCI bus • Can also function as a stand-alone processing unit in bus-less systems • 915GM chipset provides high-speed communication for GbE connectivity and graphics • Two SATA ports • Onboard memory is high-speed Double Data Rate 2 (DDR2) DRAM with access rates of up to 2 Gbps

PROCESSOR: POWERPC

Interface Concept
Website: www.interfaceconcept.com
Model: MPC7448 RSC No: 30377

MPC7448 PowerPC-based VME64x VITA 31.1 SBC • PowerPC- and PowerQUICC processor-based SBC boards (3U and 6U) • Fast Ethernet and GbE switches (up to 30 ports) • PowerPC processor- and PowerQUICC processor-based Ethernet interface controllers • Synchronous/asynchronous serial communication platforms

ACTIS Computer
Website: www.actis-computer.com
Model: CSBX-3545 RSC No: 31193

3U CompactPCI single board computer • Available for standard convection cooling or rugged conduction cooling critical embedded applications • PowerQUICC III MPC8545E up to 1.2 GHz with up to 1 GB of soldered DDR memory with ECC support • 8 MB of flash memory for the onboard monitor software • 1 GB NAND Flash for data or program storage • Includes an Altera Cyclone II FPGA offering up to 50k Logic Elements, 580 kb of RAM, and 86 embedded multipliers • The FPGA, connected to its own 64 MB of dedicated SDRAM memory, provides additional hardware computational resources to accommodate demanding applications • Two GbE ports for switched buses architectures (blades concept) and a standard 32-bit CompactPCI bus interface for local extensions • Security engine • Three-level ruggedization levels support • Linux and VxWorks RTOS support

Hunt Engineering
Website: www.hunteng.co.uk
Model: RTG004 RSC No: 30411

A USB-connected embedded PowerPC system • User-programmable Xilinx XC2VP7 FPGA with embedded PowerPC • 256 Mb of DDR SDRAM connected as two banks of 32 Mx32 @ 200 MHz • 16 Mb of flash memory for PowerPC code storage • 30 bits programmable digital I/O • High-speed (480 Mbps) USB 2.0 connection to a host PC • Can be used as a stand-alone board for embedded systems • FPGA can be configured via USB, Xilinx JTAG cable, or from onboard PROM • Single 5 V power supply required – 20 W mains power supply unit included • Hunt Engineering host API supported for Windows 2000 and XP and Linux • FPGA and DSP loading, resetting, and data exchange all performed with simple-to-use software interface • Optional expansion via HERON module slot

SHELF AND MECHANICAL COMPONENTS

Datatronics Distribution
Website: www.datatronics.com
Model: DR365-1-2 RSC No: 31626

Miniature surface mount inductors that provide effective EMI protection for applications • RoHS compliant • Ultra-thin, featuring a seated height as low as 0.047" (1.2 mm) above the printed circuit board depending on the inductance value required • Ideal for a wide range of portable, compact, and miniature devices such as PDAs, mobile phones, and portable hard drives • Wide inductance range from 3.3 µH to 100 µH (at 100 kHz, 0.1 V), with a DCR range from 0.11 to 2.8 ohms and a maximum rated current from 0.20 to 1.2 amps • Rugged operating temperature range of -20 °C to +80 °C

Crosshairs Editorial

By Chris A. Ciufo

Intel Xeons encroach on PowerPC's territory

Intel's latest crop of desktop and server CPUs is not only likely to reclaim the performance crown from rival AMD, there's also a chance they'll steal sockets from Freescale's PowerPC processors in embedded. Long a high-performance favorite for tasks such as control loops and radar processing, the MPC74xx "G4" PowerPC with AltiVec engine has been riding a success curve for more than 10 years. CompactPCI, VME, AdvancedMC, PMC, and other form factor boards rely on the PowerPC more frequently than any other General Purpose Processor (GPP) because of its stellar GFLOP benchmarks in dual- and quad-CPU configurations.

Take a look at just about any DSP board in the market and you'll likely find a PowerPC (or two) and some kind of FPGA. Current generation MPC7448 PowerPCs are just now being deployed, and I've reviewed nearly six new product announcements in the past couple of months – from vendors including Curtiss-Wright Controls Embedded Computing, Aitech, Extreme Engineering, and Momentum Computer (affiliated with Mercury Computer Systems). These companies undoubtedly chose Freescale's latest single-core PPC as next-in-line on the PowerPC road map because the current "Book E" Power Architecture scales nicely and allows some form of code migration from earlier versions that date all the way back to IBM's PowerPC 601.

But this may soon be ancient history because Intel's dual-core Xeon Ultra Low Voltage (ULV) server CPU is offering performance-per-watt numbers that rival the MPC7448. According to Mercury Computer Systems in their recent E-cast "Bringing a Quad-Core Intel Server to Embedded Applications" (www.opensystems-publishing.com/ecast), it's now possible to stuff two dual-core Xeon ULVs on a single 6U board and still be within easy reach of air- and conduction-cooling. A single Xeon ULV contains two cores running at 1.66 GHz but consumes only 15 W. This compares very favorably to a *single core* Freescale 7448 running at 1.4 GHz consuming 10 W. In effect, that second core consumes only 50 percent more power.

Moreover, while not really designed for high-end signal processing systems using Symmetrical Multiprocessor (SMP) architectures, two dual-core Xeons – unlike previous Intel CPUs such as Pentium Ms or even Intel's latest Core Duo CPU – bolt together nicely via Intel's E7520 Northbridge. According to Mercury, this configuration yields an easily programmed four-way SMP setup with 4x the previous Intel processing density *in one 6U slot* (see Figure 1). The dual-core Xeons share an onboard L2 cache while maintaining good memory bandwidth with off-chip DDR2-400 dual channel off-chip memory. Even better, the Northbridge has ample I/O, including PCI Express, which facilitates handy interboard (or internode) communication. Mercury estimates that the two CPUs, Northbridge, and SDRAM in a four-way SMP architecture would consume a total estimated 75 W on a single 6U board.

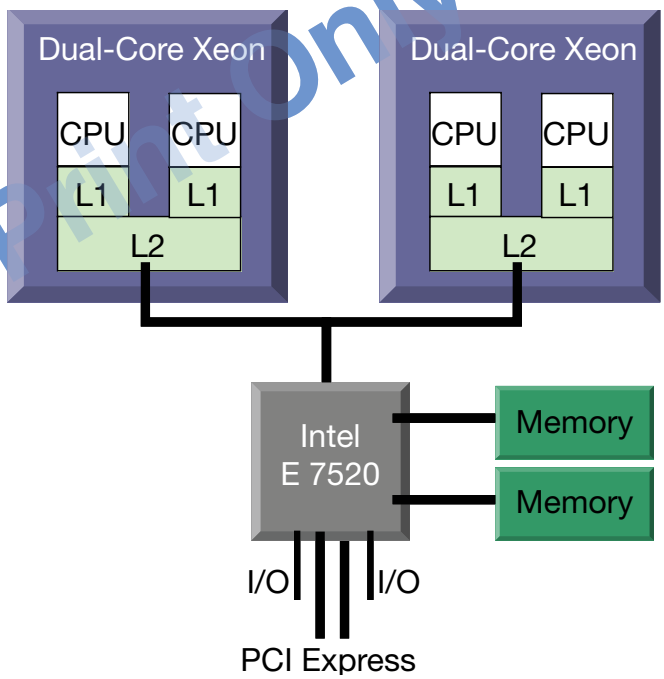
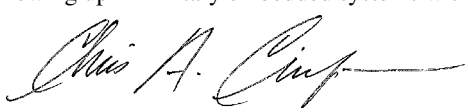


Figure 1

What's the big deal, you say? Existing PowerPC boards consume a bit less power, are ideally suited for SMP, and already have an established code base. That's true. The big deal is that the ULV Xeon is now squarely in PowerPC territory, and Intel has a road map of additional processors – including *quad cores* – that stretches out from here to eternity.

Intel is so focused on cranking out more performance-per-watt at commodity prices that embedded designers simply must consider Intel's offerings as a serious threat to the PowerPC. And when you couple the enormous code base available for Intel Architecture processors, including applications you run on your desktop, CPUs like the dual-core Xeon ULV are bound to start showing up in military embedded systems within six months.



Chris A. Ciufo
Group Editorial Director

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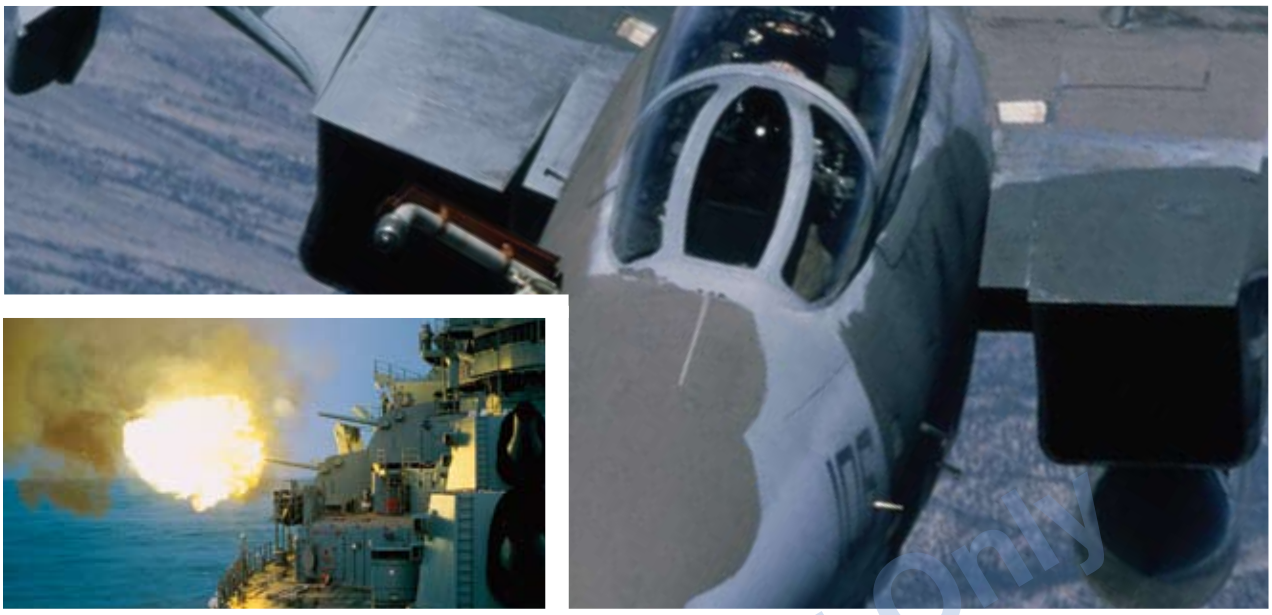

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